ESD Test Models

ESD can have serious detrimental effects on all semiconductor ICs and the system that contains them. Standards are developed to enhance the quality and reliability of ICs by ensuring all devices employed have undergone proper ESD design and testing, thereby minimizing the detrimental effects of ESD. Three major test methods are widely used in the industry today to describe uniform methods for establishing ESD-withstand thresholds (highest passing level).

They are:

Human-Body Model (HBM)

The HBM was developed to simulate the action of a human body discharging accumulated static charge through a device to ground, and employs a series RC network consisting of a 100-pF capacitor and a 1500-Ω resistor.

Machine Model (MM)

The MM simulates a machine discharging accumulated static charge through a device to ground. It comprises a series RC network of a 200-pF capacitor, and nominal series resistance of less than 1 ohm. The output waveform usually is described in terms of peak current and oscillating frequency for a given discharge voltage.

Charged-Device Model (CDM)

The CDM simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occur when there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube and hitting a metal surface. The CDM addresses the possibility that a charge may reside on a lead frame or package (e.g., from shipping) and discharge through a pin that subsequently is grounded, causing damage to sensitive devices in the path. The discharge current is limited only by the parasitic impedance and capacitance of the device. CDM testing consists of charging a package to a specified voltage, then discharging this voltage through the relevant package leads. At TI, the CDM testing is conducted using a field-induced CDM (FCDM) simulator.