Service Guide

Publication number 01680-97016
October 2005

For Safety information, Warranties, and Regulatory information, see the pages at the end of the book.

Agilent Technologies 1680/90-Series Logic Analyzer

Features

Some of the main features of the Agilent 1680A,AD-Series Logic Analyzers are as follows:

- Standalone benchtop logic analyzer
- Microsoft Windows® XP Professional operating system
- 132 data channels and 4 clock/data channels on the Agilent 1680A,AD
- 98 data channels and 4 clock/data channels on the Agilent 1681A,AD
- 64 data channels and 4 clock/data channels on the Agilent 1682A,AD
- 32 data channels and 2 clock/data channels on the Agilent 1683A,AD
- 12.1-inch LCD display
- 3.5-inch flexible disk drive
- 80GB hard disk drive
- Centronics and LAN interfaces
- IEEE 1394 interface for hosted control
- Variable setup/hold time
- 512K acquisition memory in the Agilent 1680A-series
- 2M acquisition memory in the Agilent 1680AD-series
- Marker Measurements
- PS/2 Mouse
- PS/2 keyboard support

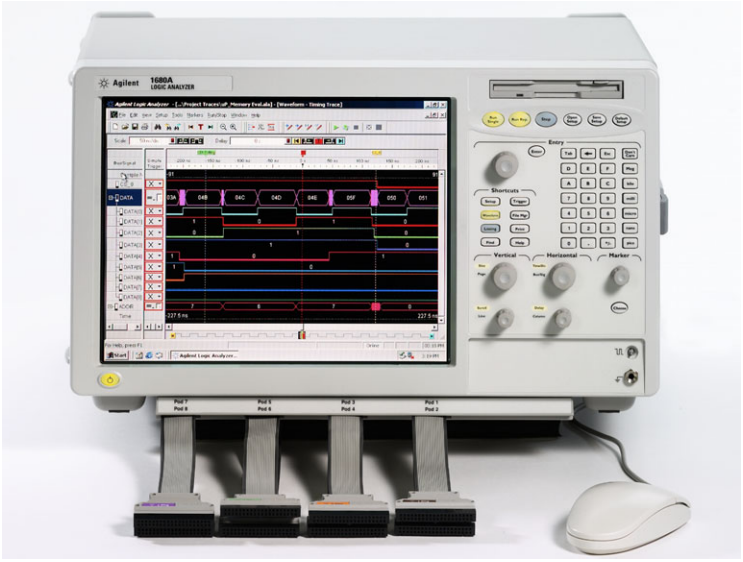
Some of the main features of the Agilent 1690A,AD-Series Logic Analyzers are as follows:

- Hosted benchtop logic analyzer
- 132 data channels and 4 clock/data channels on the Agilent 1690A,AD
- 98 data channels and 4 clock/data channels on the Agilent 1691A,AD
- 64 data channels and 4 clock/data channels on the Agilent 1692A,AD
- 32 data channels and 2 clock/data channels on the Agilent 1693A,AD
- IEEE 1394 interface for hosted control
- Variable setup/hold time
- 512K acquisition memory in the Agilent 1690A-series
- 2M acquisition memory in the Agilent 1690AD-series
- Marker Measurements

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the Agilent 1680/90-series logic analyzers.

This logic analyzer can be returned to Agilent for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for details.



Agilent Technologies 1680-Series Logic Analyzer

Agilent Technologies 1690-Series Logic Analyzer

In This Book

This book is the service guide for the Agilent 1680/90-Series Logic Analyzers and is divided into eight chapters.

Chapter 1 contains information about the logic analyzer and includes accessories, specifications and characteristics, and equipment required for servicing.

Chapter 2 tells how to prepare the logic analyzer for use.

Chapter 3 gives instructions on how to test the performance of the logic analyzer.

Chapter 4 contains calibration instructions for the logic analyzer.

Chapter 5 contains self-tests and flowcharts for troubleshooting the logic analyzer.

Chapter 6 tells how to replace assemblies of the logic analyzer and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the logic analyzer works and what the self-tests are checking.

Contents

Contents

1

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessory is supplied with the Agilent 1680/90-series logic analyzers. The part number is current as of the print date of this edition of the Service Guide, but further upgrades may change the part number. Do not be concerned if the accessory you receive has a different part number.

Accessories Supplied	Agilent Part Number	Qty
3-button Corded Mouse	1150-7845	1
Mini Keyboard	1150-7809	1

Accessories Available

For probing information, see *Probing Solutions for Logic Analysis Systems* (publication 5968-4632E) available at:

http://www.agilent.com/find/logic_analyzer_probes

Specifications

The specifications are the performance standards against which the product is tested.

Maximum State Speed (selectable)	200 MHz
Minimum Master to Master Clock Time*	5.000 ns
Threshold Accuracy	± (65 mV + 1.5% of threshold setting)

Setup/Hold Time*

Single Clock, Single Edge	4.5/-2.0 ns through -2.0/4.5 ns, adjustable in 100 ps increments
Single Clock, Multiple Edges	5.0/-2.0 ns through -1.5/4.5 ns, adjustable in 100 ps increments
Multiple Clocks, Multiple Edges	5.0/-2.0 ns through -1.5/4.5 ns, adjustable in 100 ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

Characteristics

These characteristics are not specifications, but are included as additional information.

	Full Channel	**Half Channel**
Maximum State Clock Rate	150 MHz	not applicable
Maximum Conventional Timing Rate	250 MHz	500 MHz
Memory Depth (1680A, or 1690A-series)	512 K	1024 K
Memory Depth (1680AD or 1690AD-series)	2048 K	4196 K
Channel Count		
1680A,AD or 1690A,AD	136	68
1681A,AD or 1691A,AD	102	51
1682A,AD or 1692A,AD	68	34
1683A,AD or 1693A,AD	34	17

Probes

Maximum Input Voltage ± 40V Peak AC+DC, CAT 1

Auxiliary Power

Power Through Cables 1/3 amp at 5 V maximum per cable, CAT 1

Operating Environment (for indoor use only)

Temperature:

- Instrument: 0° C to 55° C (+32° F to 131° F).
- Probe lead sets and cables: 0° C to 65° C (+32° F to 149° F).
- Disk media: 10° C to 40° C (+50° F to 104° F).

Humidity: Instrument, probe lead sets, and cables, up to 80% relative humidity at +40° C (+122° F).

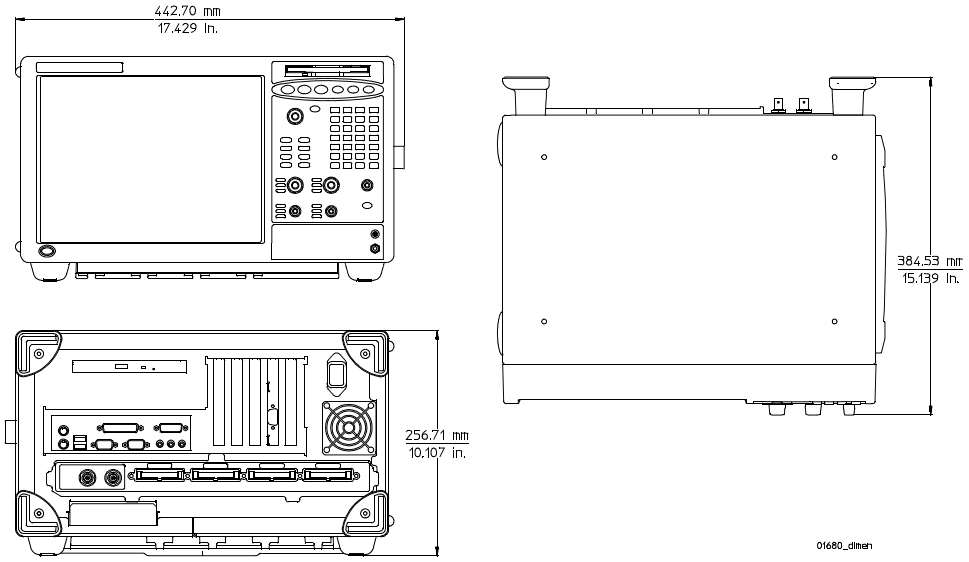
Altitude: To 3067 m (10,000 ft).

Vibration:

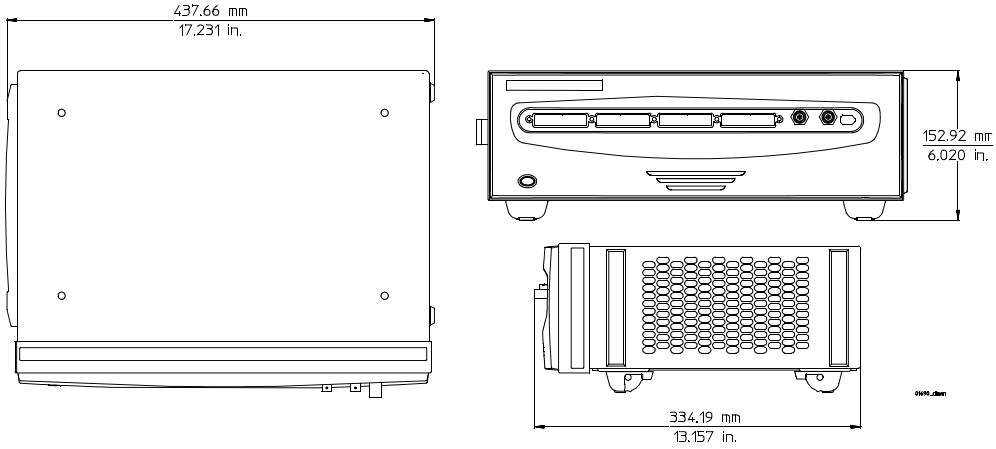
- Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, 0.3 g (rms).
- Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Dimensions

1680A,AD-Series



1690A,AD-Series



Recommended Test Equipment

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	200 MHz, 2.5 ns pulse width, <600 ps rise time	8133A Option 003	P,T
Digitizing Oscilloscope	≥6 GHz bandwidth, <58 ps rise time	54750A mainframe with 54751A plug-in module	P
Function Generator	Accuracy (5)(10^{-6}) frequency, DC offset voltage ±1.6 V	33250A	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
BNC-Banana Cable		11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
Cable	BNC (m)(m) 48 inch	8120-1840	P,T
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	1250-1200	P, T
Adapter	SMA(f)-BNC(m)	1250-2015	P
Coupler (Qty 4)	BNC (m)(m)	1250-0216	P, T
20:1 Probes (Qty 2)		54006A	P
BNC Coax Cable	BNC(m)(m), > 2 GHz bandwidth, > 1 meter length	10503A	T
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B	T
BNC Shorting Cap		1250-0774	T
BNC-Banana Adapter		1251-2277	T

*A = Adjustment P = Performance Tests T = Troubleshooting
**Instructions for making these test connectors are in chapter 3, "Testing Performance."

2

Preparing for Use

This chapter gives you instructions for preparing the logic analyzer for use.

Power Requirements

The logic analyzer requires a power source of either 115 Vac or 230 Vac, –22 % to +10 %, single phase, 48 to 66 Hz, CAT II pollution degree 2, 140/400 Watts nominal maximum power (1680A/AD-series), and 76/200 Watts nominal maximum power (1690A/AD-series).

Operating Environment

The operating environment is listed in chapter 1. The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20° C to +35° C (+68° F to +95° F)
- Humidity: 20% to 80% noncondensing

Note the recommended noncondensing humidity. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40° C to +75° C
- Humidity: Up to 90% at 65° C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

Accessories supplied with the logic analyzer are listed in “Accessories” on page 10.

3 Inspect the product for physical damage.

Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To apply power

These steps are required for all 1680A,AD and 1690A,AD-series logic analyzers.

1 Connect the power cord to the instrument and to the power source.

This instrument autodetects the line voltage from 115 VAC to 230 VAC. It is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to chapter 7, "Replaceable Parts," for option numbers of available power cables.

2 Turn on the power switch located on the front panel.

To connect the 1690A,AD-series logic analyzer to a host PC

These steps are required for the Agilent 1690A,AD-series hosted logic analyzer.

The logic analyzer user interface requires a host computer (PC) with the following characteristics (or better):

Intel Celeron, AMD K6-II 500 MHz

Windows 2000 Professional or Windows XP Professional

128MB RAM

IEEE 1394 PCI card

1 Connect one end of the 6-pin IEEE 1394 cable to the IEEE 1394 port on the host PC.

2 Connect the free end of the IEEE 1394 cable to the IEEE 1394 port on the logic analyzer.

3 Apply power to the PC if it is not turned on.

To start the user interface

Start the Agilent Logic Analyzer application from the Start menu or using a shortcut. On the desktop, the Agilent Logic Analyzer icon looks like:

Refer to the Agilent Logic Analyzer on-line help for information on how to operate the user interface. Also, refer to the window icon reference on the inside front cover of this service manual for a brief explanation of the Agilent Logic Analyzer standard icons.

To clean the logic analyzer

With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the logic analyzer. Harsh soap might damage the water-base paint.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the logic analyzer does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1.

The Logic Analyzer Interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. Provided on the inside front cover of this manual is a list of logic analyzer icons that can be referenced while performing test procedures. For more information about the logic analyzer interface, refer to the *Agilent Logic Analyzer* application's online help.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test. The examples in this chapter were performed using an Agilent 1680AD. Other analyzers in the series will have appropriate pods showing on the screen.

The performance verification procedures starting on page 3–8 are each shown from power-up. To exactly duplicate the setups in the tests, save the power-up configuration to a file on a disk, then load that file at the start of each test.

If a test fails, check the test equipment setup, check the connections, and verify adequate grounding. If a test still fails, the most probable cause of failure would be the acquisition board.

Test Interval

Test the performance of the logic analyzer against specifications at two-year intervals.

Performance Test Record

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the logic analyzer over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number. Before testing the performance of the logic analyzer, warm-up the instrument and the test equipment for 30 minutes.

To make the test connectors

The test connectors connect the logic analyzer to the test equipment.

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	1250-0698	5
100 Ω 1% resistor	0698-7212	8
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		4
20:1 Probe	54006A	2
Jumper wire		

1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip:

a Solder a jumper wire to all pins on one side of the Berg strip.

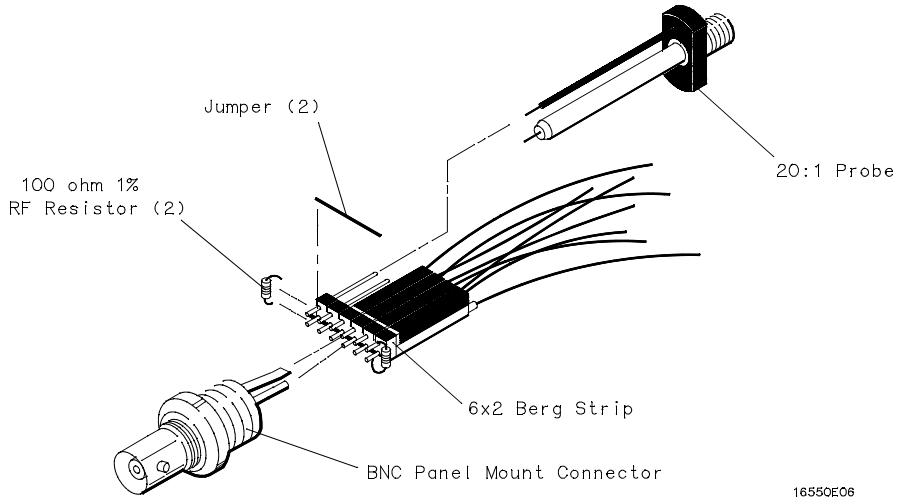
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



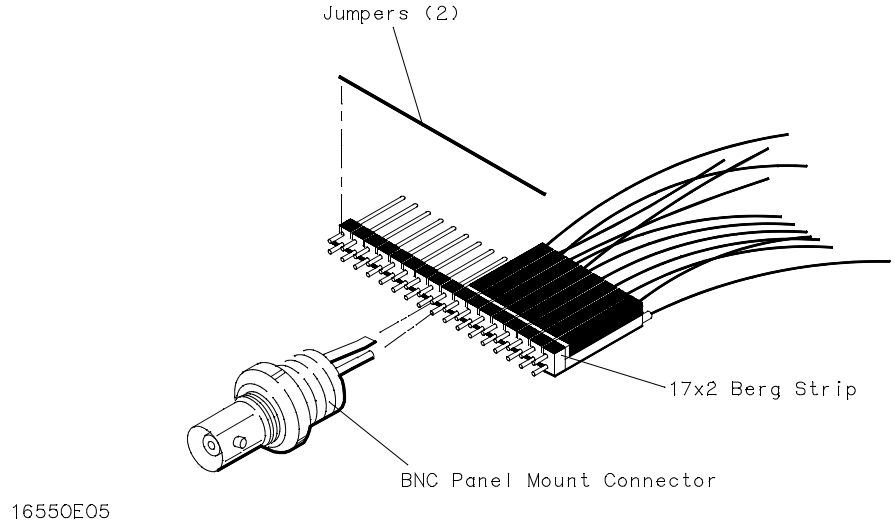
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip:

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



To set up the test equipment and the logic analyzer

Before testing the specifications of the Agilent 1680A,AD-series or 1690A,AD-series logic analyzer, the test equipment and the logic analyzer must be set up and configured.

These instructions include detailed steps for initially setting up the required test equipment and the logic analyzer. Before performing any or all of the tests in this chapter, the following steps must be done.

Equipment Required

Equipment	Critical Specifications	Recommended HP/Agilent Model/Part
Pulse Generator	200 Mhz, 2.5 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	DC offset voltage ±1.5 V	3325B Option 002

Set up the test equipment

1 Turn on the required test equipment listed in the table above. Let them warm up for 30 minutes before beginning any test.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger	Channel 1
Mode: Int Period: 5.000 ns	Mode: Pulse Divide: Pulse ÷ 2 Width: 2.500 ns Ampl: 0.80 V Offs: -1.30 V COMP: Disabled (LED Off)	Divide: Divide ÷ 2 Ampl: 0.50 V Offs: 0.00 V	Mode: Square Delay: 0.0 ps Ampl: 0.80 V Offs: -1.30 V COMP: Disabled (LED Off)

3 Set up the oscilloscope:

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	Display	Trigger	[Shift] Δ Time
Averaging: On # of averages: 16	Graticule graphs: 2	Level: 0.0 V	Stop src: channel 2 [Enter]

Channel 1	Channel 2	Define meas
External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	External Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: - 1.300 V	Thresholds: user-defined Units: Volts Upper: - 980 mV Middle: -1.30 V Lower: -1.62 V

Set up the 1680A,AD-series logic analyzer

Power-up self tests are done on the logic analyzer system components when power is applied. Any problems reported by the logic analyzer during boot must be cleared before going further. For more information, refer to Chapter 5 and Chapter 8.

1 Turn on the logic analyzer:

a Connect a keyboard and mouse to the rear panel of the logic analyzer.

b Plug in a power cord to the rear panel power connector of the logic analyzer.

c Turn on the power switch on the logic analyzer front panel.

2 Set up the logic analyzer:

a Wait for the logic analyzer boot up to complete.

b On the logic analyzer desktop, double-click the Agilent Logic Analyzer icon to launch the application.

Set up the 1690A,AD-series logic analyzer

Power-up self tests are done on the logic analyzer system components when power is applied. Logic analyzer peripheral communication tests are done when the host PC recognizes the hosted logic analyzer hardware. Any problems reported should be cleared before going further. For more information, refer to Chapter 5 and Chapter 8.

1 Connect the logic analyzer to the host PC.

2 Set up the logic analyzer:

a Wait for the logic analyzer power-up to complete.

b On the host PC desktop, double-click the Agilent Logic Analyzer icon to launch the application.

c In the Agilent Logic Analyzer application window, ensure the application reports “Online.”

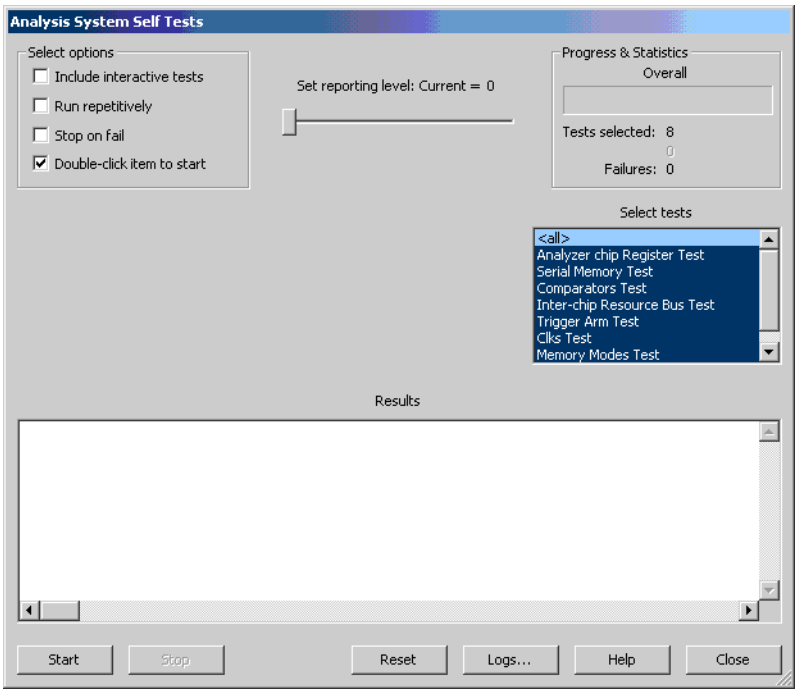
To perform the logic analyzer self-tests

The Self Test menu checks the major hardware functions of the logic analyzer to verify that it is working correctly. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analyzer, run the self-tests all at once. Refer to Chapter 8 for more information on the logic analyzer self-tests.

CAUTION: Because the most recently acquired data will be lost, be sure to save important data before running self tests.

1 In the Agilent Logic Analyzer application, choose Help>Self Test... from the main menu.

CAUTION: If you have acquired data, a warning message appears, "Running self-tests will invalidate acquired data"; click OK to continue.



2 In the Analysis System Self Tests dialog, select the self test options:

- Include interactive tests — causes interactive tests to appear in the selection lists.
- Run repetitively — runs the selected tests repetitively until you click Stop.
- Stop on fail — if you are running multiple tests or running tests repetitively, this causes the tests to stop if there is a failure.
- Double-click item to start — lets you double-click a test to start it.

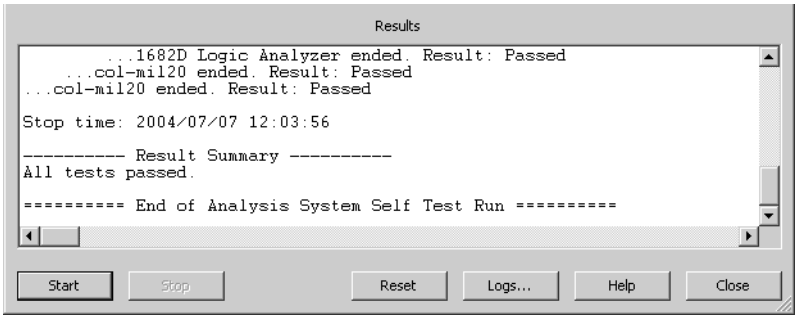
3 Set the reporting level.

Higher levels produce increasingly verbose output.

4 Select the tests you want to run.

5 Click Start.

As the tests are running, the results are reported in the lower part of the dialog and saved to a log file.



To stop running test, click Stop.

To reset the self-test options, click Reset.

To view the log file, click Logs..., select the log file you want to view, and click Open.

If, after completing the self tests, you have failures or you have questions about the performance of the logic analysis system, contact Agilent Technologies sales or support at http://www.agilent.com/find/contactus.

6 Click Close to close the Analysis System Self Tests dialog.

To test the threshold accuracy

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for pod 1, substituting the next pod for pod 1 in the instructions.

Each threshold test tells you to record a pass/fail reading in the performance test record located at the end of this chapter.

Equipment Required

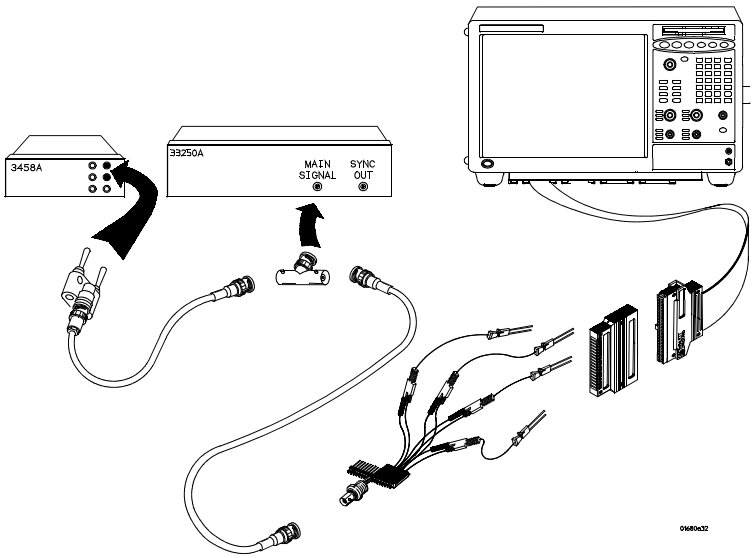
Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	Accuracy (5)(10^{-6}) frequency, DC offset voltage ±1.5 V	33250A
BNC-Banana Cable		11001-60001
BNC Tee		1250-0781
BNC Cable		8120-1840
BNC Test Connector, 17x2		

Set up the equipment

1. If you have not already done so, do the procedure “To set up the test equipment and the logic analyzer” on page 23.
2. Set up the DC source to deliver a DC voltage on the output:
   a. In the function generator Utility menu, activate the DC Level. All AC voltage functions will be disabled.
   b. Enable the high impedance load under the Output Setup menu.
3. Using a BNC-banana cable, connect the voltmeter to one side of the BNC Tee.
4. Connect the BNC Tee to the output of the DC source. Set up the logic analyzer.

Connect and configure the logic analyzer

1 Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of Pod 1 to the free side of the BNC Tee.



2 Configure the logic analyzer:

a Click the Bus/Signal Setup icon. The Analyzer Setup dialog opens.

b In the Buses/Signals tab, click Delete All at the bottom of the dialog.

c Using the mouse, activate all Pod 1 channels. Assign channels to bus/signal name My Bus 1.

Bus/Signal Name	Channels Assigned	Width	Pod 2 Threshold: TTL (1.50 V)	Pod 1 Threshold: TTL (1.50 V)
My Bus 1	Pod 1[15:0]	16		✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓ ✓

d Scroll the channel assignments to the left. Assign the clock/data channel for the Pod 1 (that is, C1) to My Bus 1.

Bus/Signal Name	Channels Assigned	Width	Clocks	Pod 8 Threshold: TTL (1.50 V)	Pod 7 Threshold: TTL (1.
My Bus 1	Clocks[C1],	17	✓		

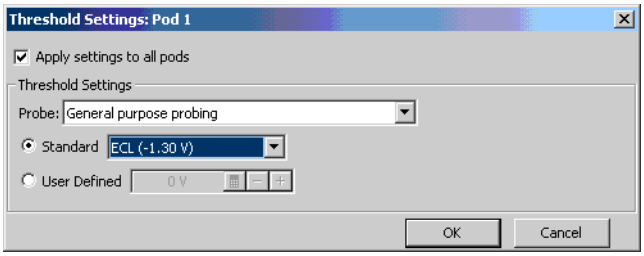
3 Activate the DC source output.

Test the ECL Threshold

1 Set up the logic analyzer:

a In the Analyzer Setup dialog, click the threshold field for Pod 1. The Threshold Settings dialog appears.

b In the Threshold Settings dialog, select Standard and ECL (–1.30 V).



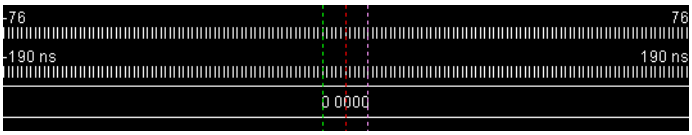
c Click OK to close the Threshold Settings dialog.

d Click OK to close the Analyzer Setup dialog.

2 Test the high-to-low transition:

a On the DC source, enter a voltage setting of –1.384 V.

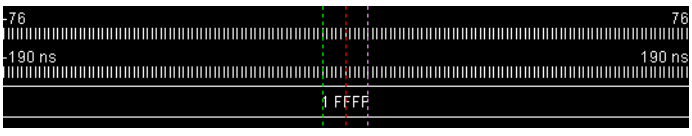
b On the logic analyzer, click the Run icon. The display should show all channels at a logic "0".



3 Test the low-to-high transition:

a On the DC source, enter a voltage setting of –1.216 V.

b On the logic analyzer, click the Run icon. The display should show all channels at a logic "1" (0x1FFFF).



4 Record a PASS/FAIL in the performance test record for Threshold Accuracy Pod 1 - ECL.

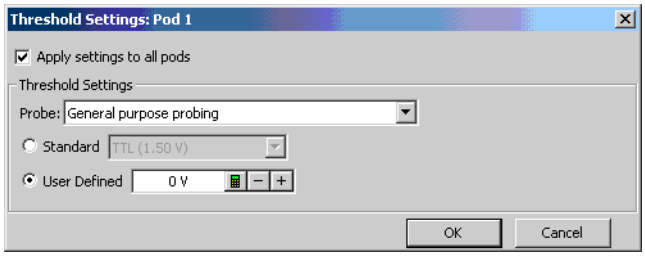
Test the 0 V User Threshold

1 Set up the logic analyzer:

a On the logic analyzer, click the Bus/Signal Setup icon. The Analyzer Setup dialog opens.

b In the Analyzer Setup dialog, click the threshold field for Pod 1. The Threshold Settings dialog appears.

c In the Threshold Settings dialog, select User Defined and enter 0 V in the associated field.



d Click OK to close the Threshold Settings dialog.

e Click OK to close the Analyzer Setup dialog.

2 Test the high-to-low transition:

a On the DC source, enter a voltage setting of –0.064 V.

b On the logic analyzer, click the Run icon. The display should show all channels at a logic "0".

3 Test the low-to-high transition:

a On the DC source, enter a voltage setting of 0.064 V.

b On the logic analyzer, click the Run icon. The display should show all channels at a logic "1" (0x1FFFF).

4 Record a PASS/FAIL in the performance test record for Threshold Accuracy Pod 1 - User 0 V.

Test the next pod

1 Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator until all pods have been tested.

2 Start with “Connect and configure the logic analyzer” on page 29 substituting the next pod to be tested for pod 1.

To set up the logic analyzer for the state mode tests

1 Set up the logic analyzer:

a If you have not already done so, do the procedure "To set up the test equipment and the logic analyzer" on page 23.

b Exit and restart the Agilent Logic Analyzer application to reinitialize the logic analyzer.

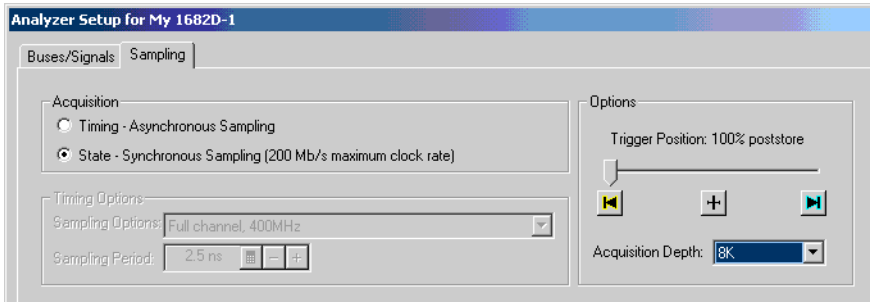
2 Configure the Analyzer Setup dialog:

a Click the Sampling Setup icon.

b Select State - Synchronous Sampling.

c Configure Trigger Position - 100% poststore.

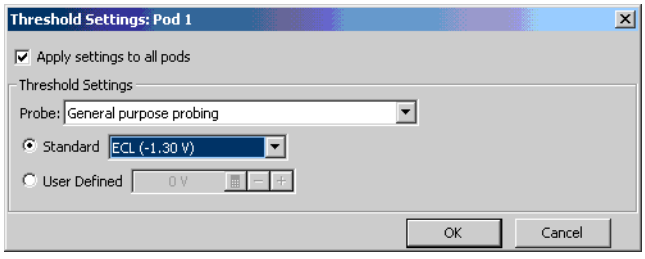
d Select an Acquisition Depth of 8K.



e Click the Buses/Signals tab.

f Click the threshold field of one of the pods. The Threshold Settings dialog appears.

g In the Threshold Settings dialog, select Standard and ECL (–1.30 V).



h Click OK to close the Threshold Settings dialog.

i Click OK to close the the Analyzer Setup dialog.

3 Configure the trigger according to your logic analyzer:

a In the Listing window, click on the trigger pattern field for My Bus 1 to select.

b Enter the following pattern for your logic analyzer.

1680A,AD, 1690A,AD - "AA"

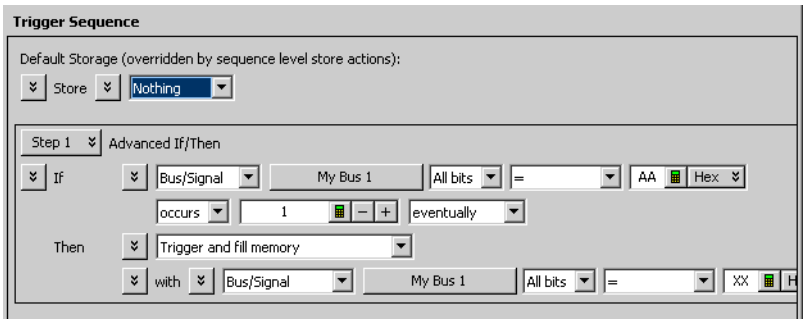
1681A,AD, 1691A,AD - "2A"

1682A,AD, 1692A,AD - "AA"

1683A,AD, 1693A,AD - "A"

c Click the Trig Trigger Setup icon.

d For the Default Storage, select Store Nothing.



e Click OK to close the Advanced Trigger dialog.

4 Activate the pulse generator data and clock outputs:

a On the pulse generator, enable the channel 1 OUTPUT, channel 1 $\overline{\text{OUTPUT}}$, channel 2 OUTPUT and channel 2 $\overline{\text{OUTPUT}}$ (LEDs off)

b On the pulse generator, enable the trigger OUTPUT. (LED off)

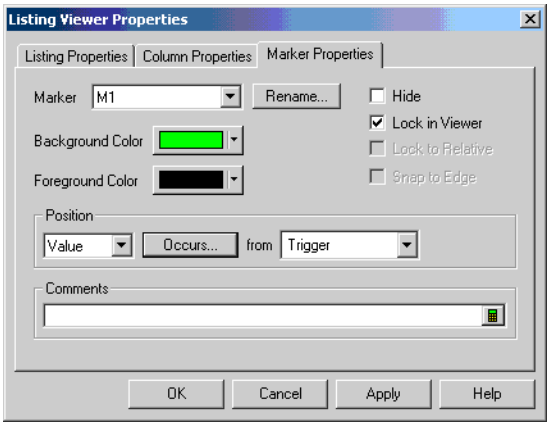
5 Set up the Markers:

The following procedure is done after the first run of test data is acquired (during one of the state clock mode tests).

a From the main menu, choose Markers>Properties....

b In the Marker Properties tab of the Listing Viewer Properties dialog,

select the M1 marker.



c In the Position box, select Value.

d Click on the Occurs... button and the Value dialog appears.

e Click on the Find occurrences field, and enter 4096.

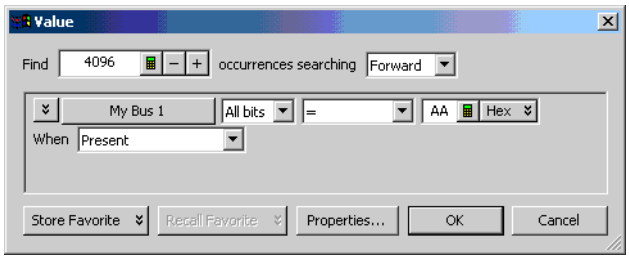
f Click on the pattern field, then enter the following pattern according to the logic analyzer being tested:

1680A,AD, 1690A,AD - "AA"

1681A,AD, 1691A,AD - "2A"

1682A,AD, 1692A,AD - "AA"

1683A,AD, 1693A,AD - "A"



g Click OK to close the Value dialog.

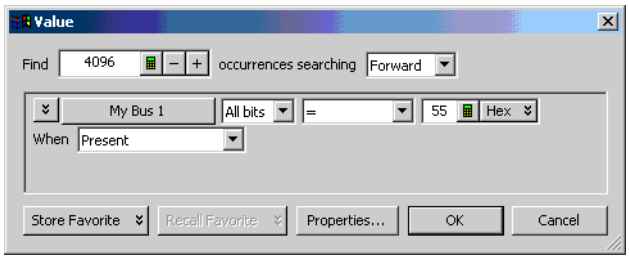
h Repeat steps b through f to configure marker M2 using the following pattern according to the logic analyzer being tested.

1680A,AD, 1690A,AD - "55"

1681A,AD, 1691A,AD - "15"

1682A,AD, 1692A,AD - "55"

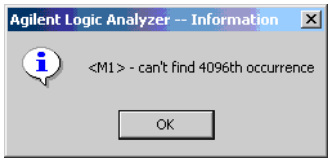
1683A,AD, 1693A,AD - "5"



i Click OK to close the Value dialog.

j In the Listing Viewer Properties dialog, select Beginning Of Data in the "from" field.

The logic analyzer markers are now configured to verify the test data. If the error message "can't find 4096 occurence(s)" does not appear, the test passes. Click OK to close the Listing ViewerProperties dialog



When the above error message appears, one or more samples of test data is incorrect. When this happens, check the following and attempt the test again:

- All cables are properly connected.
- Configuration of each test equipment is correct.
- Logic analyzer is properly set up according to the test procedure.

To test the single-clock, single-edge, state acquisition

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for single-clock, single-edge, state acquisition.

This test checks two combinations of data channels using a single-edge clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	200 MHz 2.5 ns pulse width, <600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥6 GHz bandwidth, <58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

If you have not already done so, do the following procedures:

“To set up the test equipment and the logic analyzer” on page 23.

“To set up the logic analyzer for the state mode tests” on page 33.

Connect and configure the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.

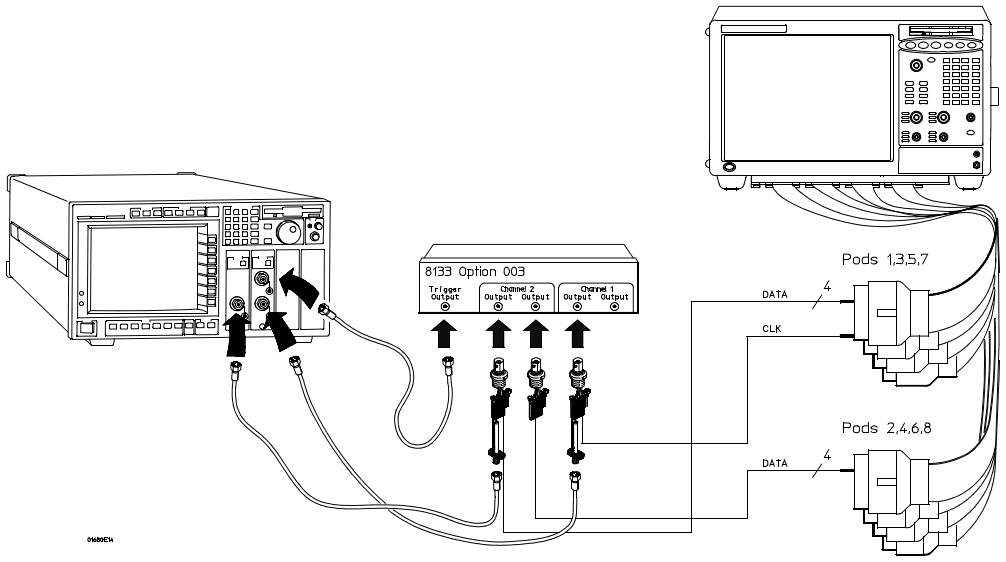
If you are testing a 1680/81/90/91A,AD, you will repeat this test for the second combination.

2 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trigger Output.

Connect the 1680/81/90/91A,AD Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	Pod 1 clock/data channel (Clk 1)
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11*	Pod 1 clock/data channel (Clk 1)

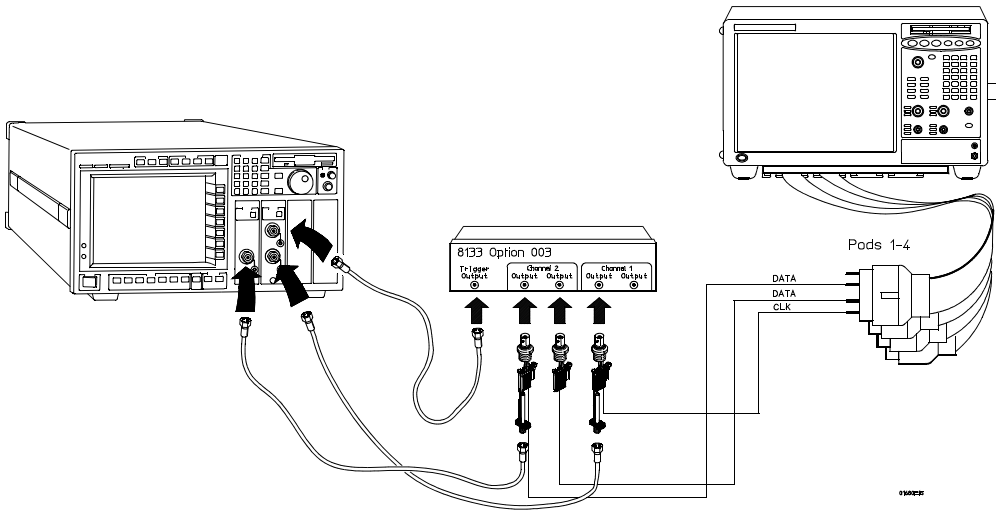
*1680A,AD or 1690A,AD only



Connect the 1682/83/92/93A,AD Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11* Pod 4, channel 11*	Pod 1 clock/data channel (Clk 1)

*1682A,AD or 1692A,AD only.

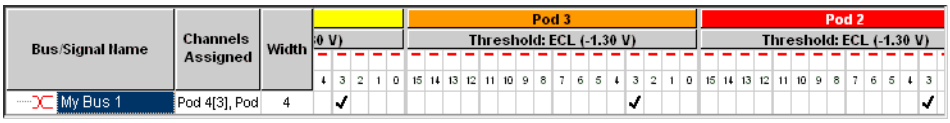


3 Activate the data channels that are connected according to one of the previous tables:

a Click on the Bus/Signal Setup icon. The Analyzer Setup dialog opens.

b In the Buses/Signals tab, click Delete All at the bottom of the dialog.

c Using the mouse, activate the data channels being tested. Assign channels to bus/signal name My Bus 1.



d Click OK to close the Analyzer Setup dialog.

Verify the test signal

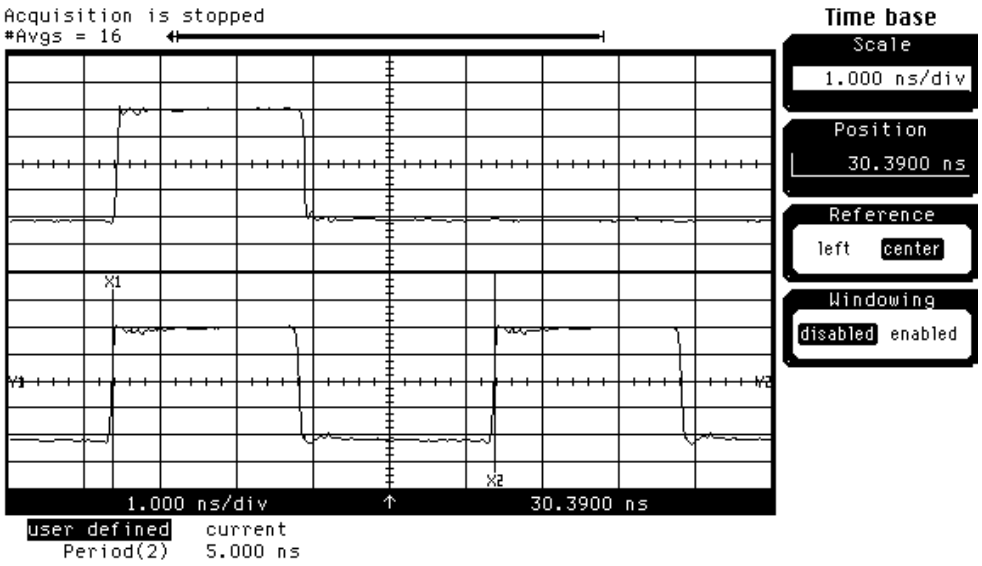
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 5.000 ns, +0 ps or –100 ps:

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 5.000 ns, go to step d. If the period is less than 5.000 ns, go to step 2.

d In the oscilloscope Timebase menu, increase Position 5.000 ns. If the period is not less than 5.000 ns, decrease the pulse generator Period in until one of the two periods measured is less than 5.000 ns.

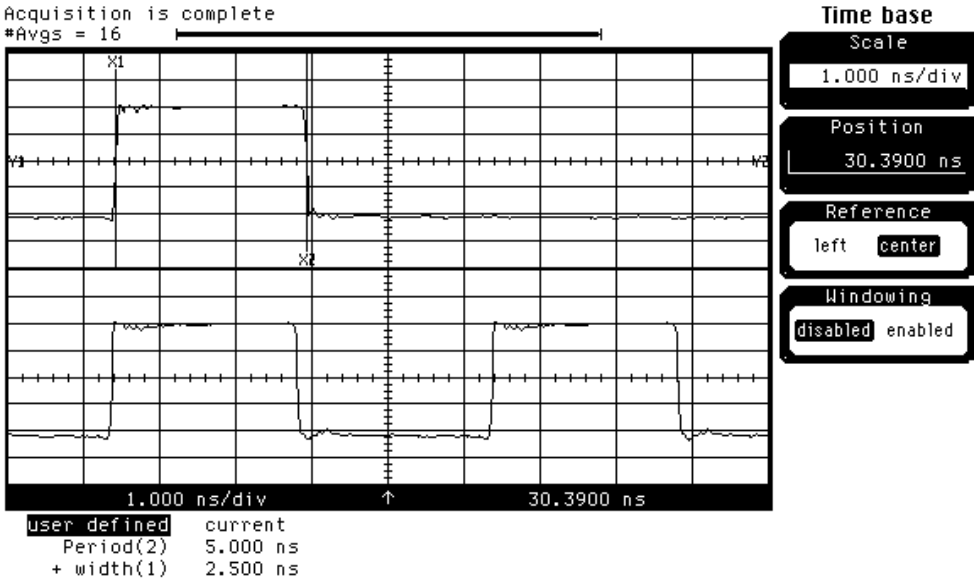


2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 2.500 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

The following setup/hold combinations will be tested:

Setup/Hold Combinations

Test Combination	Setup/Hold Times	Setup/Hold Window	Sample Position (in middle of Window)
1	4.50/-2.0 ns	2.5 ns	-3.25 ns
2	-2.0/4.50 ns	2.5 ns	+3.25 ns

1 Disable the pulse generator channel 1 COMP (with the LED off).

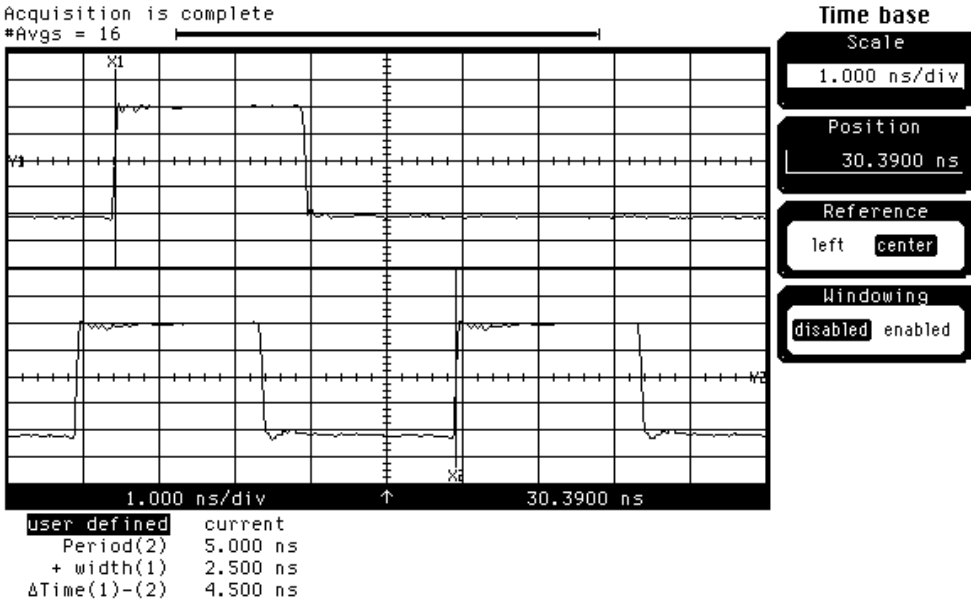
2 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps as measured on the oscilloscope:

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising, Edge number 2.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the data waveform so the falling edge is near the center of the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

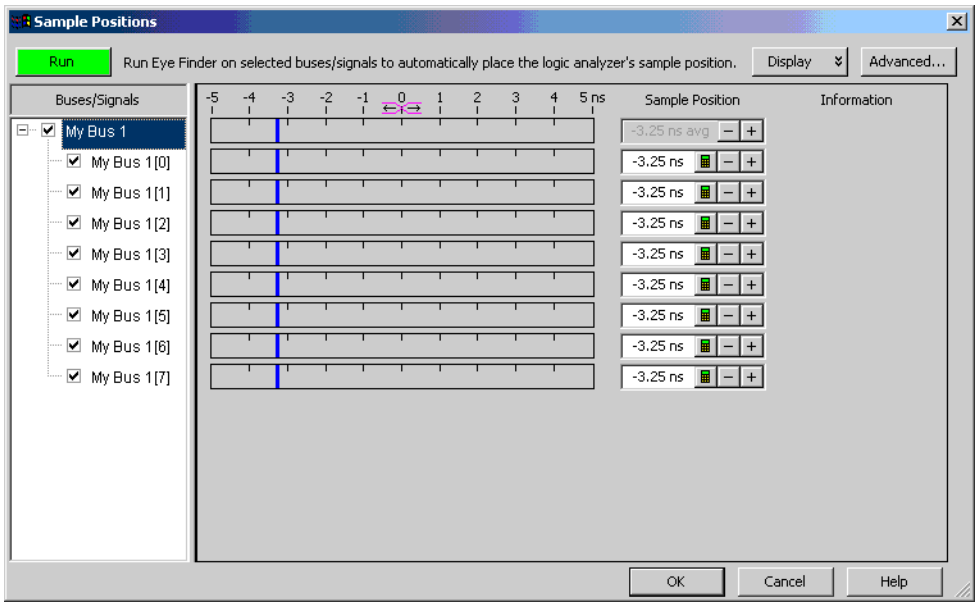


3 Select the logic analyzer sample positions:

a Click the Sampling Setup icon. The Analyzer Setup dialog opens with the Sampling tab displayed.

b Click Sample Positions....

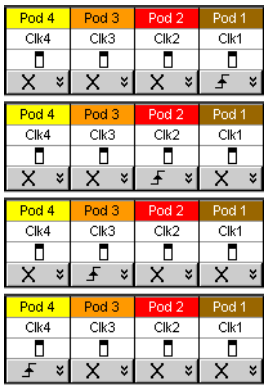
c In the Sample Positions dialog, drag the blue bar for My Bus 1 to the sample position of the first setup/hold combination to be tested (or enter the value in the signal fields).



d Click OK to close the Sample Positions dialog.

4 Select the clock to be tested:

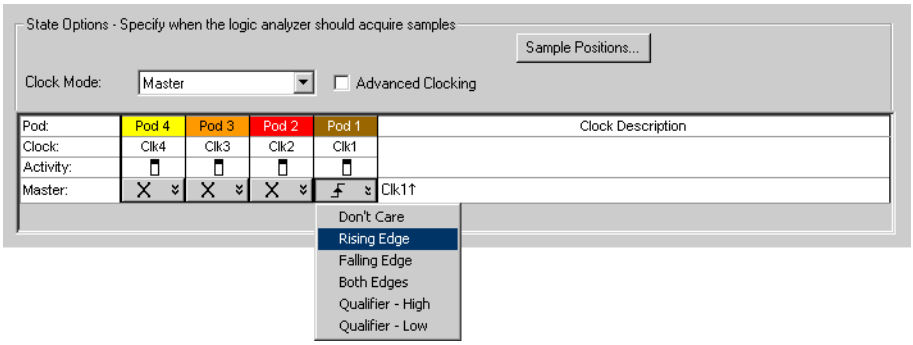
The following clock configurations will be used in steps 4, 5, and 6.



a In the Analyzer Setup dialog, click on the Sampling tab.

b In the Sampling tab, click the Master button for the first clock to be tested (Clk 1) and select Rising Edge.

c Click the Master buttons for the remaining clocks and select Don't Care to turn off the other clocks.



d Connect the clock to be tested to the pulse generator channel 1 output.

e Click OK to close the Analyzer Setup dialog.

5 Verify the test data:

a Click the Run icon.

b If you have not already done so, do “Set up the Markers:” on page 34.

c If the "can't find 4096 occurence(s)" message does not appear, the test passes.

The test passes when the logic analyzer finds all occurances of the patterns programmed into the Markers. If the test passes, record a "Pass" in the performance test record under single-clock single-edge next to the clock and edge being tested.

6 Test the next clock:

a Click on the Sampling Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 4, 5, and 6 for the next clock configuration listed in step 4 until all listed clock combinations have been tested.

7 Enable the pulse generator channel 1 COMP (with the LED on).

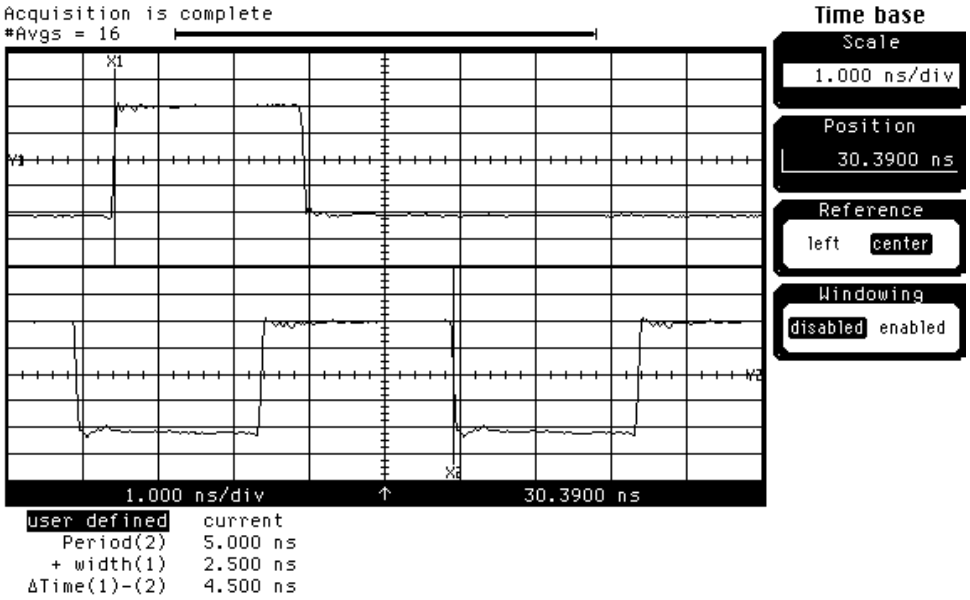
8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps as measured on the oscilloscope:

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1,

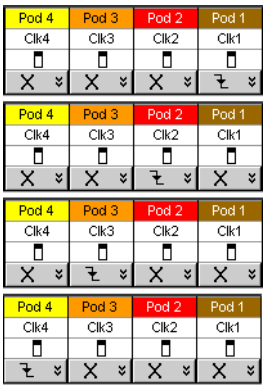
then select [Enter] to display the setup time (Δ Time(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.



9 Select the clock to be tested:

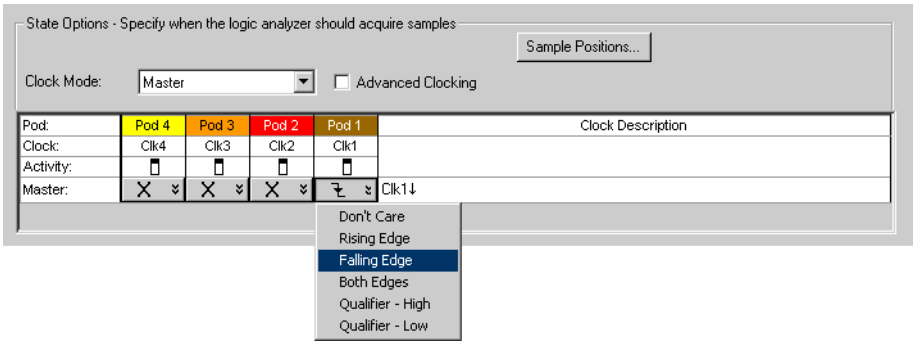
The following clock configurations will be used in steps 9, 10 and 11.



a In the Analyzer Setup dialog, click the Sampling tab.

b In the Sampling tab, click the Master button for the first clock to be tested (Clk 1) and select Falling Edge.

c Click the Master buttons for the remaining clocks and select Don't Care to turn off the other clocks.



d Connect the clock to be tested to the pulse generator channel 1 output.

e Click OK to close the Analyzer Setup dialog.

10 Verify the test data:

a Click the Run icon.

b If you have not already done so, do “Set up the Markers:” on page 34.

c If the "can't find 4096 occurence(s)" message does not appear, the test passes.

The test passes when the logic analyzer finds all occurances of the patterns programmed into the Markers. If the test passes, record a "Pass" in the performance test record under single-clock single-edge next to the clock and edge being tested.

11 Test the next clock:

a Click the Sampling Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 9, 10, and 11 for the next clock configuration listed in step 9 until all listed clock combinations have been tested.

12 Test the next setup/hold combination:

a Click the Bus/Signal Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 1 through 12 for the next setup/hold combination listed on page 41.

Test the next channels (1680/81A,AD and 1690/91A,AD)

Connect the next combination of data channels and clock channels; then, test them.

Start with “Connect and configure the logic analyzer” on page 37, connect the next combination; then, continue through the complete test.

To test the multiple-clock state acquisition

Testing the multiple-clock, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for multiple-clock, state acquisition.

This test checks two combinations of data using multiple clocks at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	200 MHz 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 If you have not already done so, do the following procedures:

"To set up the test equipment and the logic analyzer" on page 23.

"To set up the logic analyzer for the state mode tests" on page 33.

2 Increase the pulse generator channel 2 width to 3.000 ns.

Connect and configure the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.

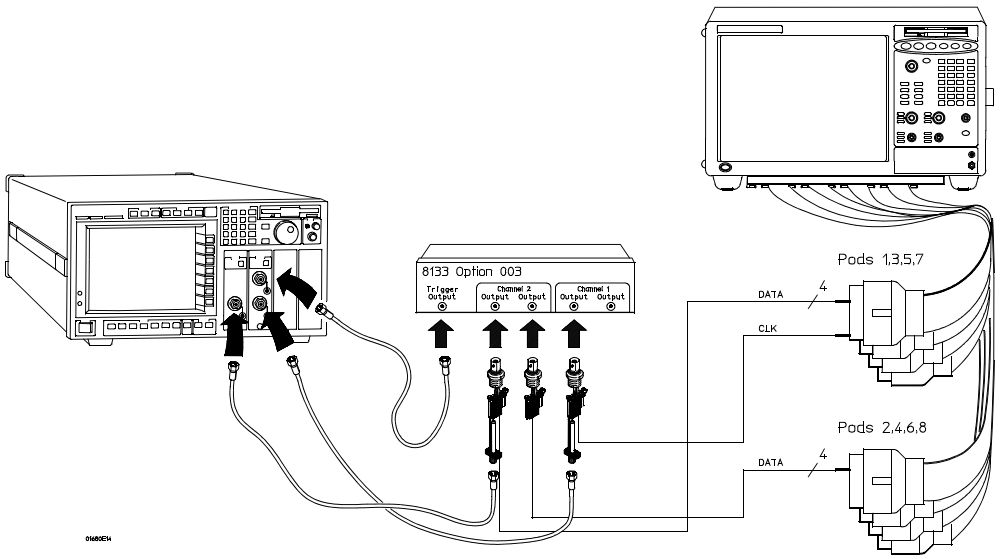
If you are testing a 1680/81/90/91A,AD, you will repeat this test for the second combination.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the 1680/81/90/91A,AD Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	Clock/data channel for Pod 1, 2, 3, and 4 (Clk 1, Clk 2, Clk 3, Clk 4)
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11 *	Clock/data channel for Pod 1, 2, 3, and 4 (Clk 1, Clk 2, Clk 3, Clk 4)

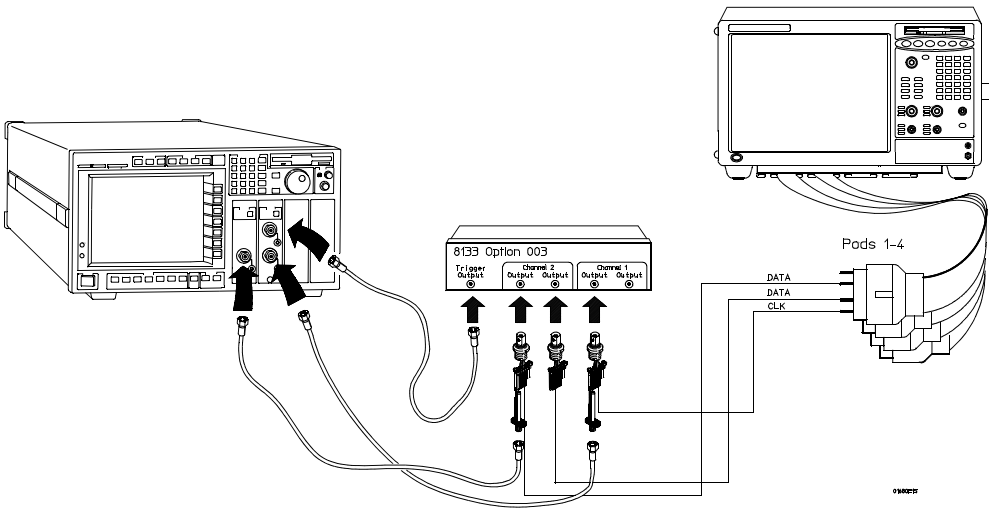
*1680A, AD or 1690A, AD only.



Connect the 1682/83/92/93A,AD Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11 * Pod 4, channel 11 *	Clock/data channel for Pod 1, 2, 3, and 4 (Clk 1, Clk 2, Clk 3, Clk 4)

*1682A, AD or 1692A, AD only.

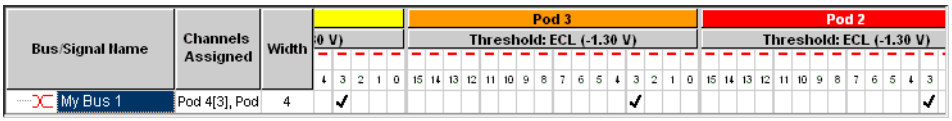


3 Activate the data channels that are connected according to one of the previous tables:

a Click the Bus/Signal Setup icon. The Analyzer Setup dialog opens.

b Under the Buses/Signals tab, click Delete All at the bottom of the dialog.

c Using the mouse, activate the data channels being tested. Assign channels to bus/signal name My Bus 1.



d Click OK to close the Analyzer Setup dialog.

Verify the test signal

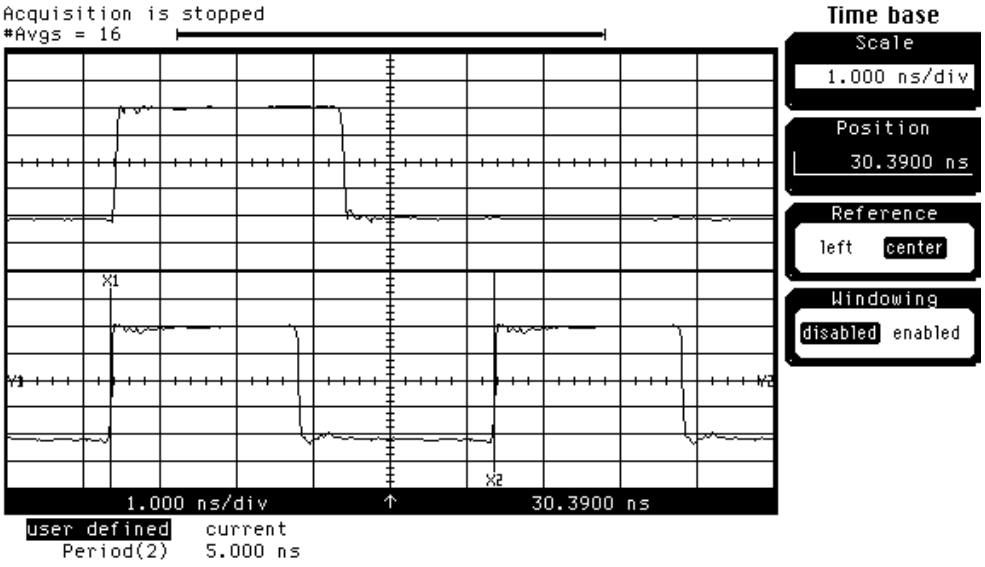
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 5.000 ns, +0 ps or –100 ps:

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 5.000 ns, go to step d. If the period is less than 5.000 ns, go to step 2.

d In the oscilloscope Timebase menu, increase Position 5.000 ns. If the period is not less than 5.000 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 5.000 ns.

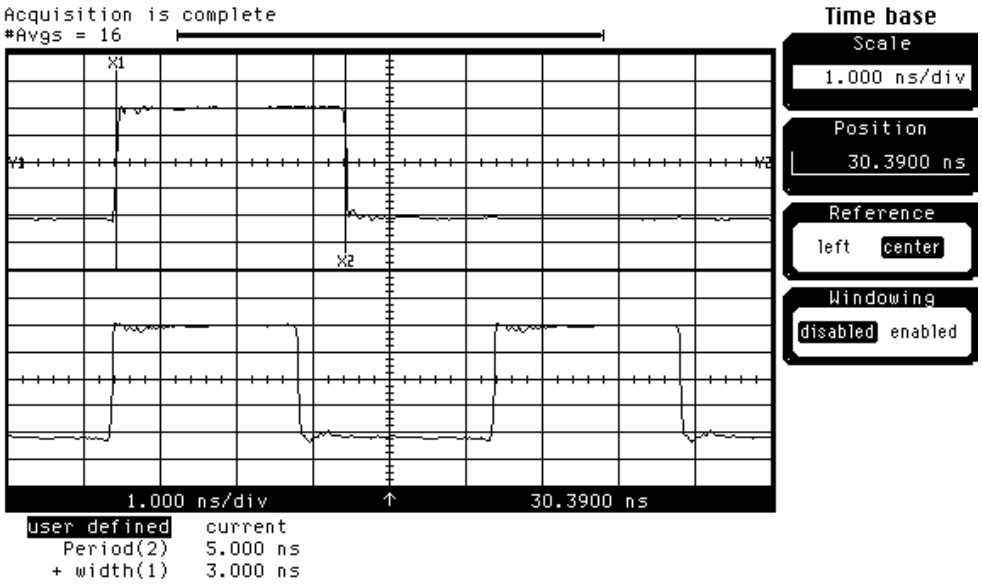


2 Check the data pulse width. Using the oscilloscope verify that the data pulse width is 3.000 ns, +0 ps or –100 ps:

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

The following setup/hold combinations will be tested.

Setup/Hold Combinations

Test Combination	Setup/Hold Times	Setup/Hold Window	Sample Position (in middle of Window)
1	5.0/-2.0 ns	3.0 ns	-3.5 ns
2	-1.5/4.50 ns	3.0 ns	+3.0 ns

1 Disable the pulse generator channel 1 COMP (LED off).

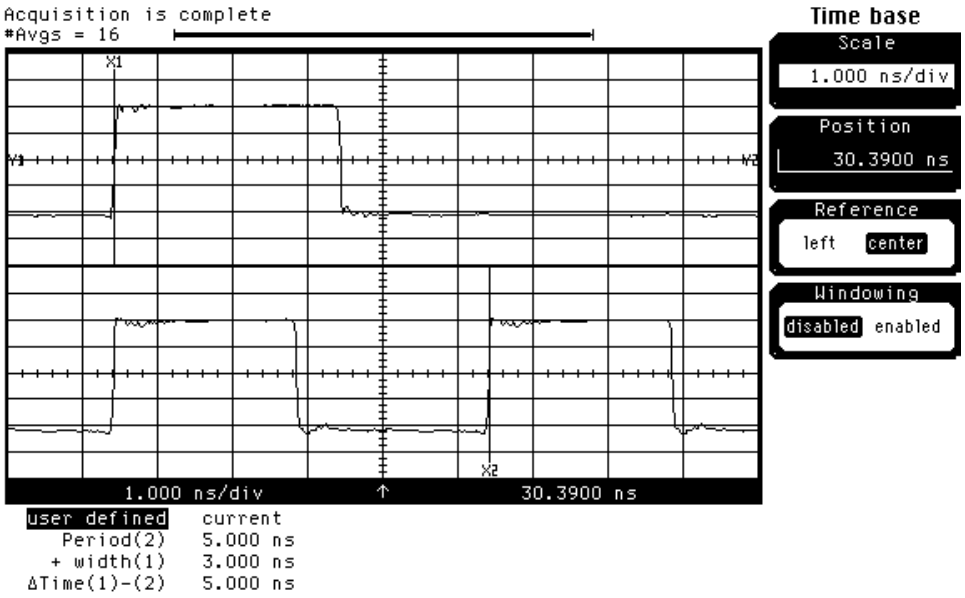
2 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps as measured on the oscilloscope:

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising, Edge number 2.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the data waveform so the falling edge is near the center of the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

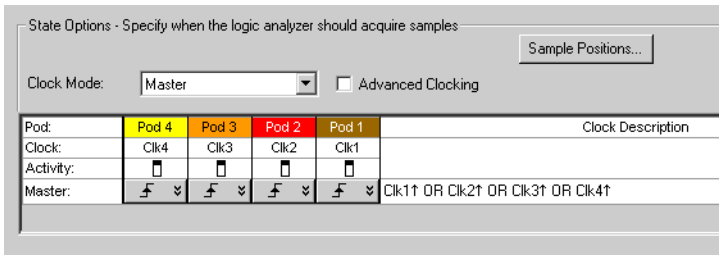


3 Select the clocks to be tested:

a Click the Sampling Setup icon. The Analyzer Setup dialog opens.

b In the Sampling tab, click the Master button for one of the clocks and select Rising Edge.

c Repeat the above steps for each of the remaining clocks until all clocks have been configured with Rising Edge.



d Connect all clock channels to the pulse generator channel 1 output.

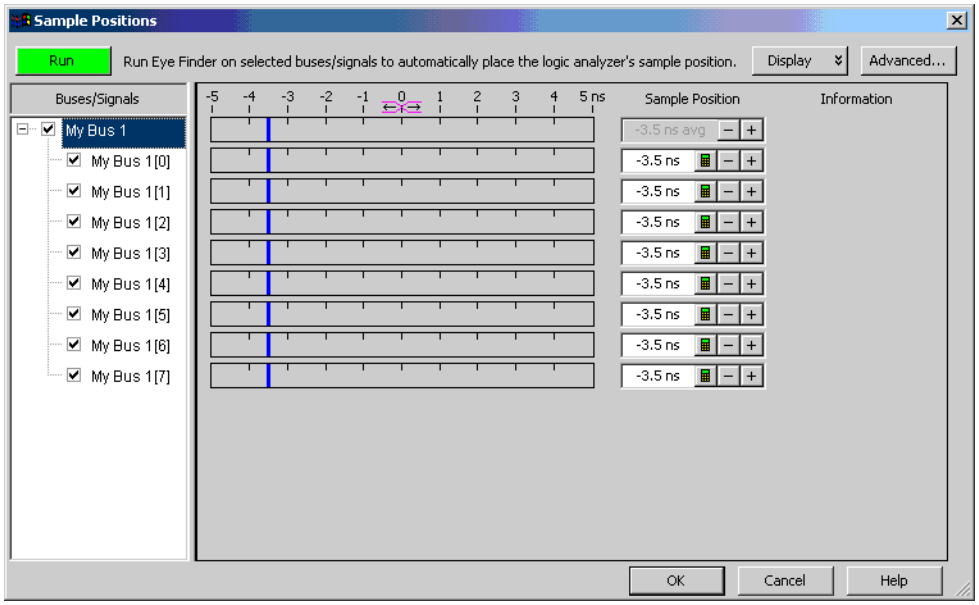
e Click OK to close the Analyzer Setup dialog.

4 Select the logic analyzer sample positions:

a Click the Sampling Setup icon. The Analyzer Setup dialog opens with the Sampling tab displayed.

b Click Sample Positions....

c In the Sample Positions dialog, drag the blue bar for My Bus 1 to the sample position of the first setup/hold combination to be tested (or enter the value in the signal fields).



d Click OK to close the Sample Positions dialog.

5 Verify the test data:

a Click the Run icon.

b If you have not already done so, do “Set up the Markers:” on page 34.

c If the "can't find 4096 occurence(s)" message does not appear, then the test passes.

The test passes when the logic analyzer finds all occurances of the patterns programmed into the Markers. If the test passes, record a "Pass" in the performance test record under single-clock single-edge next to the clock and edge being tested.

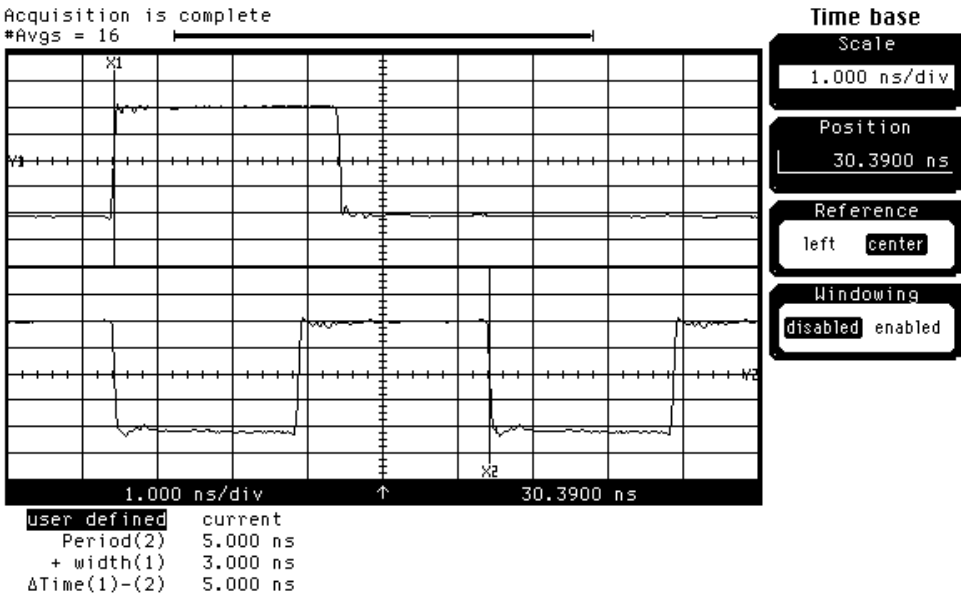
6 Enable the pulse generator channel 1 COMP (with the LED on).

7 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or –100 ps:

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.



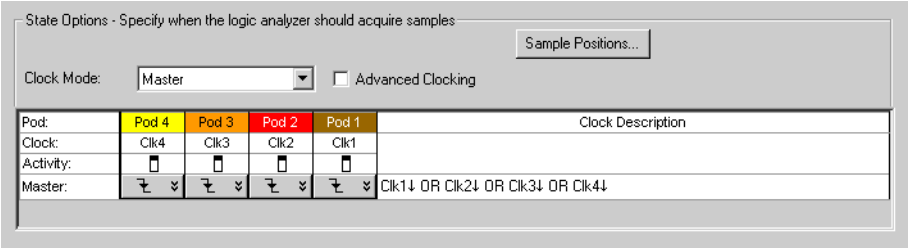
8 Select the clocks to be tested:

a Click the Sampling Setup icon. The Analyzer Setup dialog opens.

b In the Sampling tab, click the Master button for one of the clocks and select Falling Edge.

c Repeat the above steps for each of the remaining clocks until all clocks

have been configured with Falling Edge.



d Click OK to close the Analyzer Setup dialog.

9 Verify the test data:

a Click the Run icon.

b If you have not already done so, do “Set up the Markers:” on page 34.

c If the "can't find 4096 occurence(s)" message does not appear, the test passes.

The test passes when the logic analyzer finds all occurances of the patterns programmed into the Markers. If the test passes, record a "Pass" in the performance test record under single-clock single-edge next to the clock and edge being tested.

10 Test the next setup/hold combination:

a Click the Bus/Signal Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 1 through 10 for the next setup/hold combination listed in step 1 in page 52.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels (1680/81A, AD and 1690/91A, AD)

Connect the next combination of data channels and clock channels, then repeat the previous test.

Start with “Connect and configure the logic analyzer” on page 49, connect the next combination, then continue through the complete test.

To test the single-clock, multiple-edge, state acquisition

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time.
- Maximum state acquisition speed.
- Setup/Hold time for single-clock, multiple-edge, state acquisition.

This test checks two combinations of data using a multiple-edge single clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	200 MHz 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 If you have not already done so, do the following procedures:

"To set up the test equipment and the logic analyzer" on page 23

"To set up the logic analyzer for the state mode tests" on page 33

2 Modify the following pulse generator settings:

Period: 10.000 ns

Channel 2: Width 3.000 ns

Channel 2: Pulse ÷1

Channel 1: Pulse

Channel 1: Width 5.000 ns

Connect and configure the logic analyzer

1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.

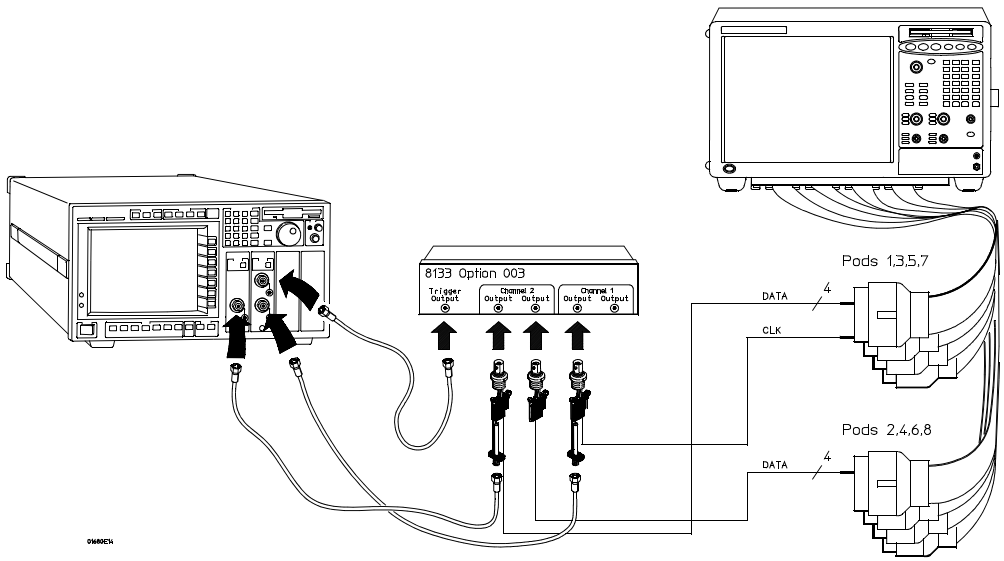
If you are testing a 1680/81/90/91A,AD, you will repeat this test for the second combination.

2 Using the SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the 1680/81/90/91A,AD Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	Pod 1 clock/data channel (Clk1)
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11 *	Pod 1 clock/data channel (Clk1)

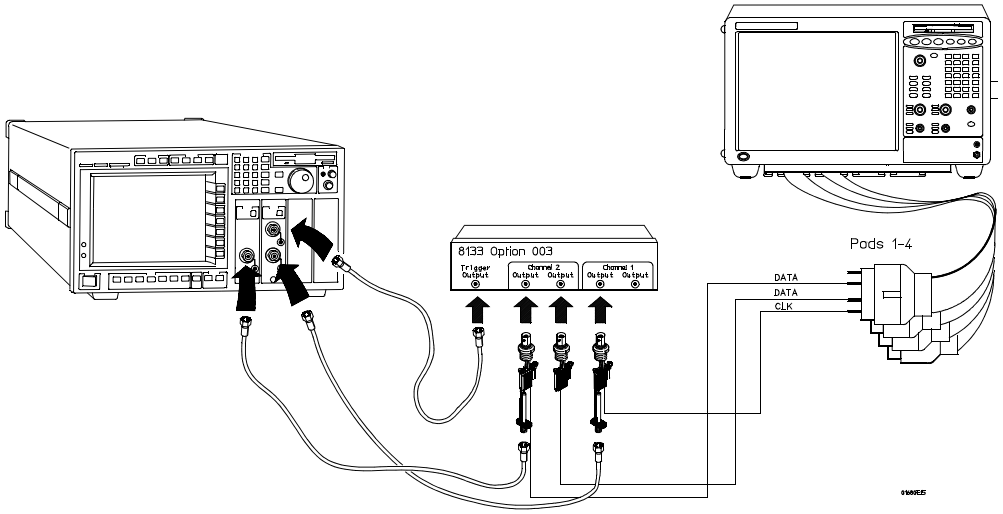
*1680A,AD or 1690A,AD only.



Connect the 1682/83/92/93A,AD Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 * Pod 4, channel 3 *	Pod 1 clock/data channel (Clk1)

*1682A,AD or 1692A,AD only.

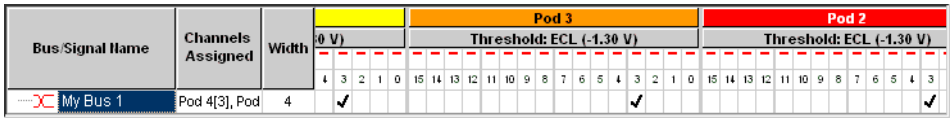


3 Activate the data channels that are connected according to one of the previous tables:

a Click the Bus/Signal Setup icon. The Analyzer Setup dialog opens.

b In the Buses/Signals tab, click Delete All at the bottom of the dialog.

c Using the mouse, activate the data channels being tested. Assign channels to bus/signal name My Bus 1.



d Click OK to close the Analyzer Setup dialog.

Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 5.000 ns, +0 ps or –100 ps:

a Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).

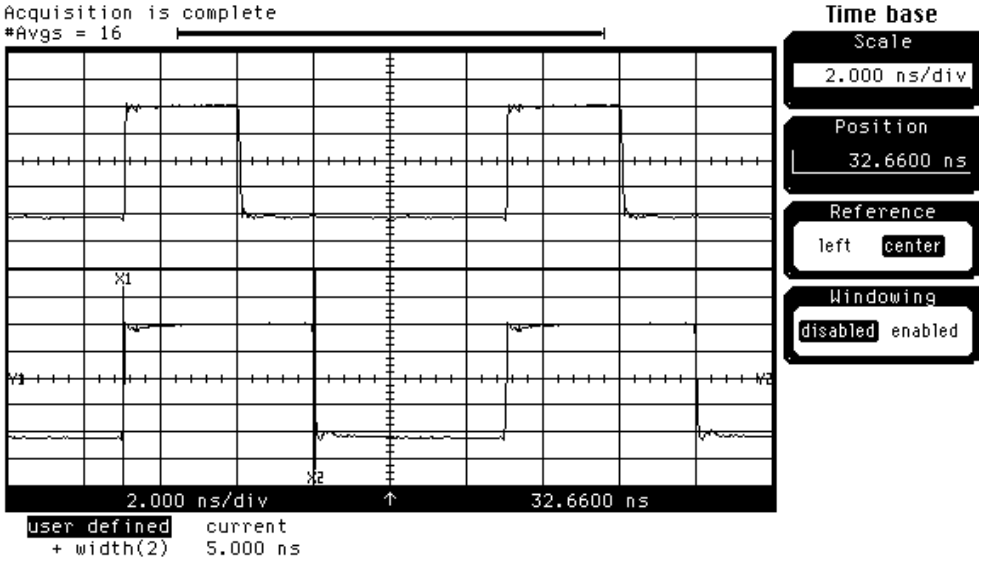
b In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 5.000 ns, go to step e. If the positive-going pulse width is less than or equal to 5.000 ns but greater than 4.900 ns, go to step 2.

e On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 5.000 ns but greater than 4.900 ns, go to step 2.

f Adjust the pulse generator Period and Channel 1 width until the oscilloscope + width (2) or - width (2) reads less than or equal to 5.000 ns, but greater than 4.900 ns.



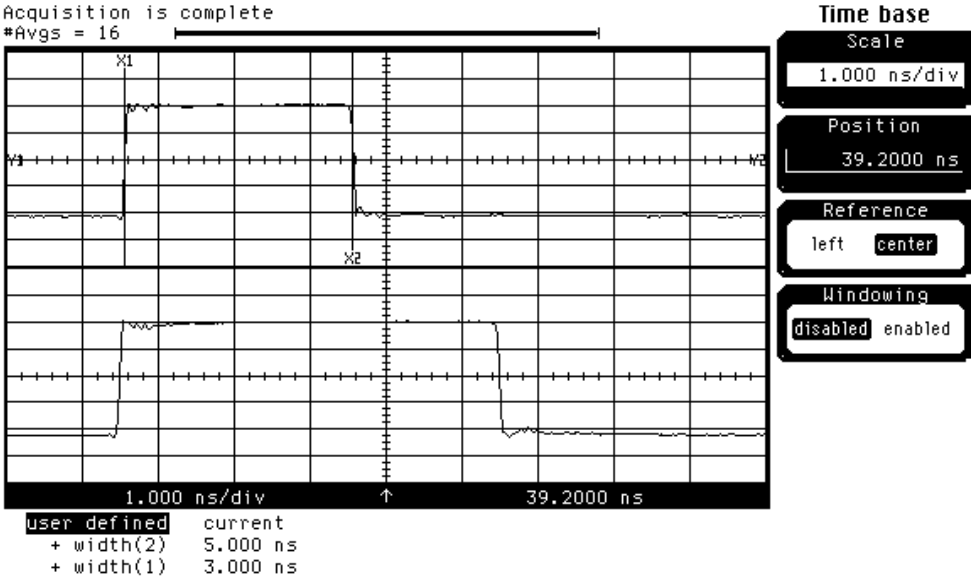
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.000 ns, +0 ps or –100 ps:

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

The following setup/hold combinations will be tested.

Setup/Hold Combinations

Test Combination	Setup/Hold Times	Setup/Hold Window	Sample Position (in middle of Window)
1	5.0/-2.0 ns	3.0 ns	-3.5 ns
2	-1.5/4.50 ns	3.0 ns	+3.0 ns

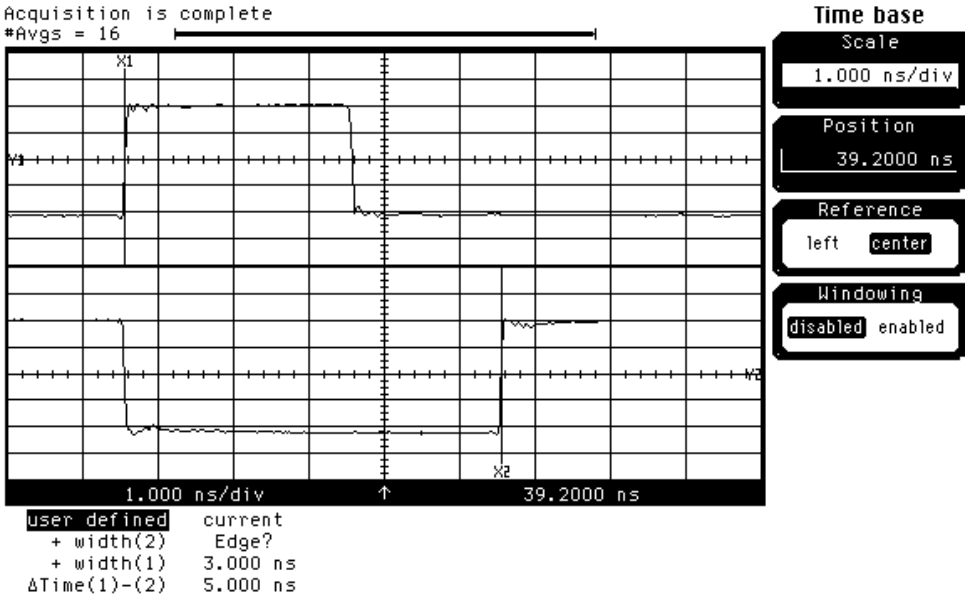
1 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps:

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is near the center of the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 2 Delay until the pulses are aligned according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

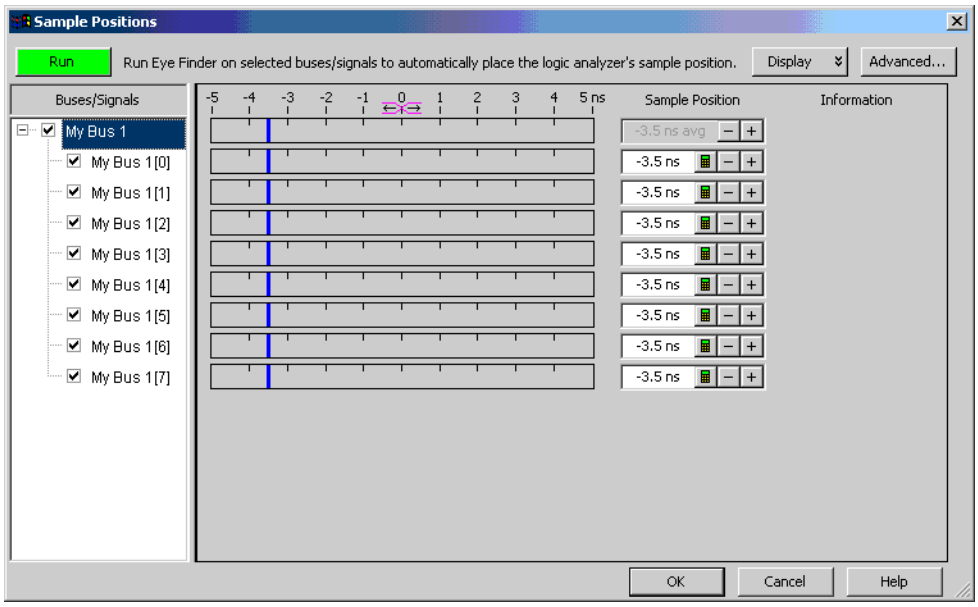


2 Select the logic analyzer sample positions:

a Click the Sampling Setup icon. The Analyzer Setup dialog opens with the Sampling tab displayed.

b Click Sample Positions....

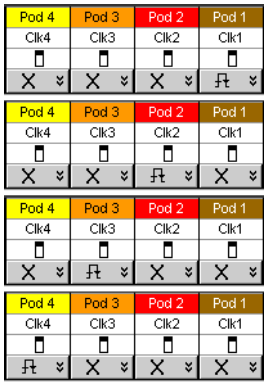
c In the Sample Positions dialog, drag the blue bar for My Bus 1 to the sample position of the first setup/hold combination to be tested (or enter the value in the signal fields).



d Click OK to close the Sample Positions dialog.

3 Select the clock to be tested:

The following clock configurations will be used in steps 3, 4, and 5.

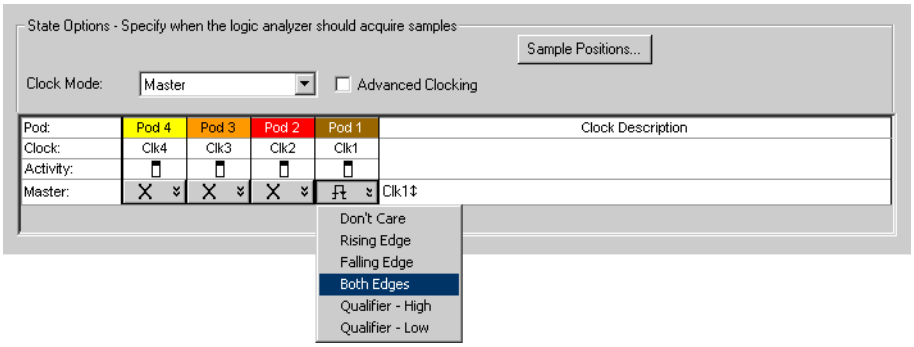


a In the Analyzer Setup dialog, click the Sampling tab.

b In the Sampling tab, click the Master button for the first clock to be tested (Clk 1) and select Both Edges.

c Click the Master buttons for the remaining clocks and select Don't Care

to turn off the other clocks.



d Connect the clock to be tested to the pulse generator channel 1 output.

e Click OK to close the Analyzer Setup dialog.

4 Verify the test data:

a Click the Run icon.

b If you have not already done so, do “Set up the Markers:” on page 34.

c If the "can't find 4096 occurence(s)" does not appear, then the test passes.

The test passes when the logic analyzer finds all occurrences of the patterns programmed into the Markers. If the test passes, record a "Pass" in the performance test record under single-clock single-edge next to the clock and edge being tested.

5 Test the next clock:

a Click the Sampling Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 3, 4, and 5 for the next clock configuration listed in step 4 until all listed clock combinations have been tested.

6 Test the next setup/hold combination:

a Click the Bus/Signal Setup icon.

b Disconnect the clock just tested from the pulse generator.

c Repeat steps 1 through 6 for the next setup/hold combination listed in step 1 in page 61.

Test the next channels (1680/81A,AD and 1690/91A,AD)

Connect the next combination of data channels and clock channels, then repeat the previous test.

Start with “Connect and configure the logic analyzer” on page 58, connect the next combination, then continue through the complete test.

To test the time interval accuracy

Testing the time interval accuracy does not check a specification, but does check the following:

- 125 MHz oscillator

This test verifies that the 125 MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	200 MHz 2.5 ns pulse width, < 600 ps rise time	8133A option 003
Function Generator	Accuracy≤ (5)(10^{-6}) x frequency	33250A
SMA Cable		8120-4948
Adapter	BNC(m)-SMA(f)	1250-2015
BNC Test Connector, 6x2		

Set up the equipment

1 Set up the logic analyzer:

a If you have not already done so, do the procedure “To set up the test equipment and the logic analyzer” on page 23.

b Exit and restart the Agilent Logic Analyzer applications to reinitialize the logic analyzer.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 1	Trigger
Mode: Ext	Mode: Square	Divide: Divide ÷ 1
	Delay: 0.000 ns	Ampl: 0.50 V
	High: -0.90 V	Ampl: 0.50 V
	Low: -1.70 V	Offs: 0.00V
	COMP: Disabled (LED off)	

3 Set up the function generator according to the following table.

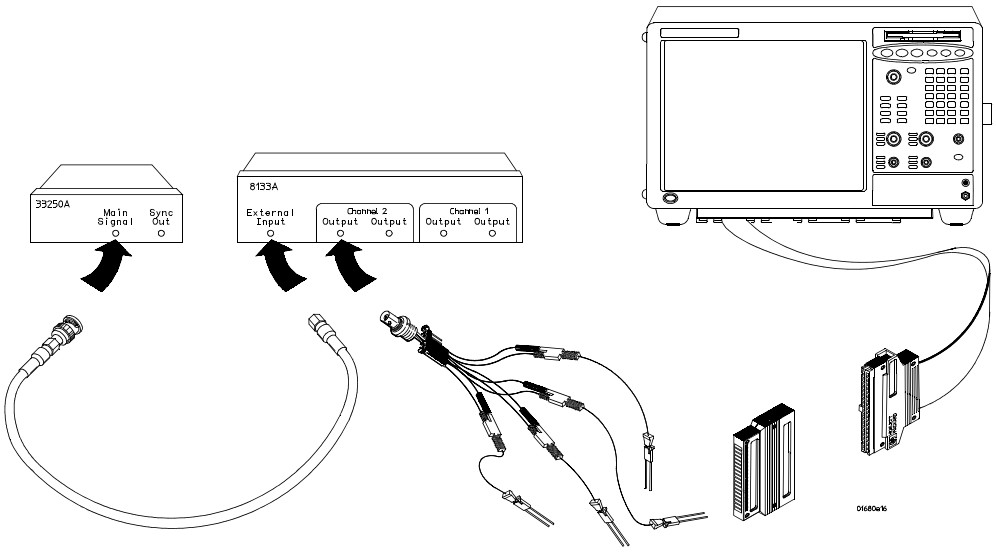
Function Generator Setup

Freq:	40.000 MHz
Ampl:	1.00 Vpp
Offset:	0.0 mV
Modulation	Off

Connect and configure the logic analyzer

1 Using a 6-by-2 test connector, connect channel 0 of Pod 1 to the pulse generator channel 1 output.

2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



3 Enable the function generator output and the pulse generator Channel 1 output.

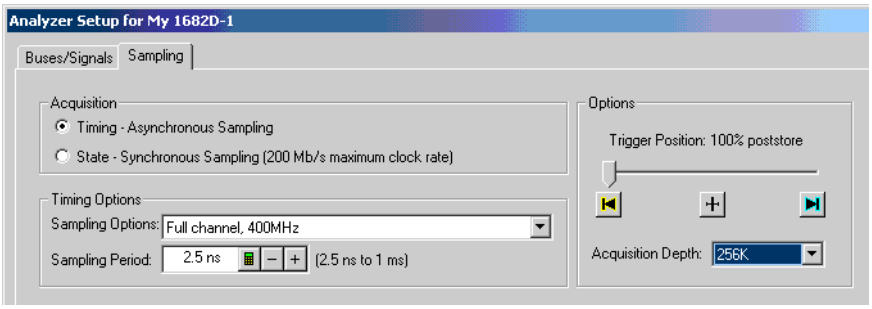
4 Configure the Analyzer Setup dialog:

a Click the Sampling Setup icon.

b In the Analyzer Setup dialog, select Timing - Asynchronous Sampling.

c Configure Trigger Position - 100% poststore.

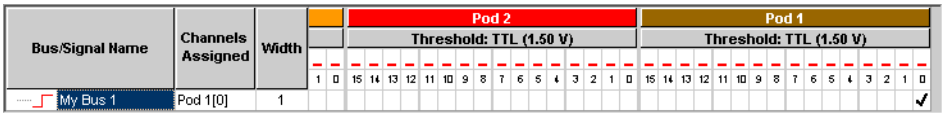
d Select an Acquisition Depth of 256K.



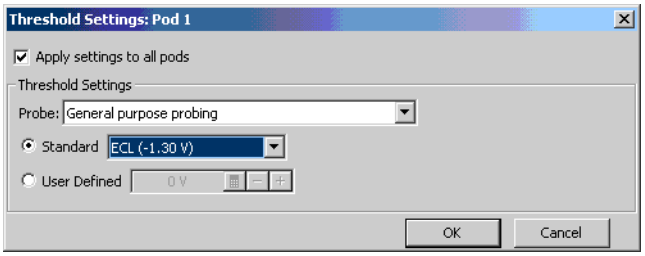
5 Configure the logic analyzer channels:

a Click the Buses/Signals tab. In the Buses/Signals tab, click Delete All at the bottom of the dialog.

b Using the mouse, select Pod 1 channel 0 to activate the channel.



c Click the threshold field for Pod 1. In the Threshold Settings dialog, select Standard and ECL (–1.30).



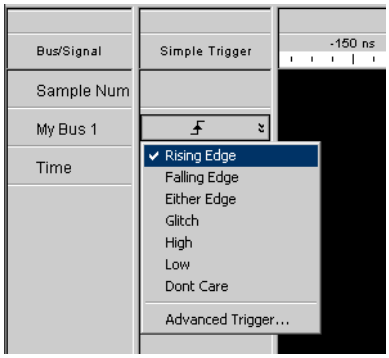
d Click OK to close the Threshold Settings dialog.

e Click OK to close the Analyzer Setup dialog.

6 Set up the trigger in the Waveform window:

a Select the Simple Trigger field next to bus/signal name My Bus 1.

b In the pop-up menu, select Rising Edge.



Acquire and verify the test data

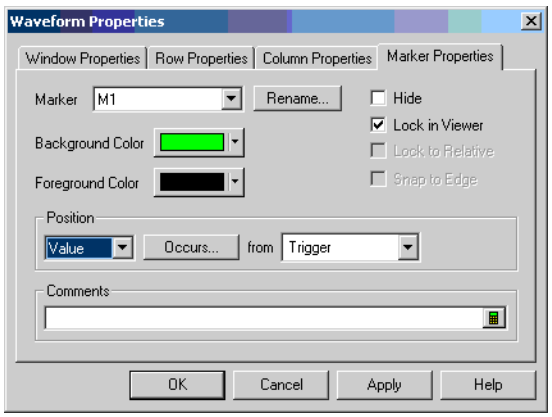
1 Click the Run icon to fill acquisition memory.

2 Set up the M1 marker for time interval measurement:

a From the main menu, choose Markers>Properties....

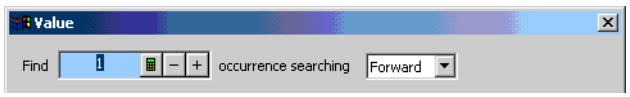
b In the Marker Properties tab of the Waveform Properties dialog, select the M1 marker.

c In the Position box, select Value.



d Click Occurs....

e In the Value dialog, enter “1” in the Find occurrences field.



f Click OK to close the Value dialog.

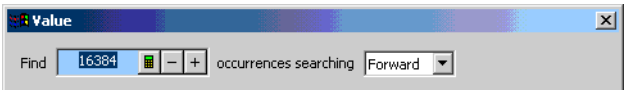
3 Set up the M2 marker for time interval measurement:

a In the Marker Properties tab of the Waveform Properties dialog, select the M2 marker.

b In the Position box, select Value.

c Click Occurs....

d In the Value dialog, enter “16384” in the Find occurrences field.

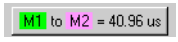


e Click OK to close the Value dialog.

f In the Position box, select M1 in the “from” field. The Position should now read Value Occurs from M1.

g Click Apply; then, click OK to close the Waveform Properties dialog.

4 An Interval Measurement should already be visible in the Markers Toolbar. If not, choose Markers>New Time Interval Measurement from the main menu; in the Time Interval dialog, select from M1 to M2, and click OK. An M1 to M2 time interval field should now be visible in the Markers Toolbar.



5 Click on the Run-Repetitive icon. Allow the logic analyzer to acquire data for at least 100 runs, as reported at the bottom of the window. Observe the M1 to M2 time interval field in the Markers Toolbar and ensure the time interval field is between 40.95571 and 40.96429 µs during the test.

Performance Test Record

Agilent 1680/90-Series Logic Analyzer_____

Serial No._____ Work Order No._____

Recommended Test Interval - 2 Years/4000 hours Date_____

Recommended next testing_____ Temperature_____

Test	Settings	Results	
Self-Tests		Pass/Fail	_____
Threshold Accuracy	± (65 mV + 1.5% of threshold setting)		
Pod 1	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 2	ECL, ±84mV	Pass/Fail	_____
	0 V, ± 65mV	Pass/Fail	_____
Pod 3	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 4	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 5	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 6	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 7	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____
Pod 8	ECL, ±84 mV	Pass/Fail	_____
	0 V, ±65 mV	Pass/Fail	_____

Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.5/-2.0 ns	Clk 1↑ Clk 2↑ Clk 3↑ Clk 4↑	_____ _____ _____ _____	Clk 1↓ Clk 2↓ Clk 3↓ Clk 4↓	_____ _____ _____ _____
	Setup/Hold Time	-2.0/4.5 ns	Clk 1↑ Clk 2↑ Clk 3↑ Clk 4↑	_____ _____ _____ _____	Clk 1↓ Clk 2↓ Clk 3↓ Clk 4↓	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	4.5/-2.0 ns	Clk 1↑ Clk 2↑ Clk 3↑ Clk 4↑	_____ _____ _____ _____	Clk 1↓ Clk 2↓ Clk 3↓ Clk 4↓	_____ _____ _____ _____
	Setup/Hold Time	-2.0/4.5 ns	Clk 1↑ Clk 2↑ Clk 3↑ Clk 4↑	_____ _____ _____ _____	Clk 1↓ Clk 2↓ Clk 3↓ Clk 4↓	_____ _____ _____ _____
Multiple-Clock, Multiple-Edge Acquisition						
				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	5.0/-2.0 ns	Clk 1↑ + Clk 2↑ + Clk 3↑ + Clk 4↑	_____	Clk 1↓ + Clk 2↓ + Clk 3↓ + Clk 4↓	_____
	Setup/Hold Time	-1.5/4.5 ns	Clk 1↑ + Clk 2↑ + Clk 3↑ + Clk 4↑	_____	Clk 1↓ + Clk 2↓ + Clk 3↓ + Clk 4↓	_____
All Pods, Channel 11	Setup/Hold Time	5.0/-2.0 ns	Clk 1↑ + Clk 2↑ + Clk 3↑ + Clk 4↑	_____	Clk 1↓ + Clk 2↓ + Clk 3↓ + Clk 4↓	_____
	Setup/Hold Time	-1.5/4.5 ns	Clk 1↑ + Clk 2↑ + Clk 3↑ + Clk 4↑	_____	Clk 1↓ + Clk 2↓ + Clk 3↓ + Clk 4↓	_____

Performance Test Record (continued)

Test	Settings		Results	
Single-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)	
				Pass/Fail
All Pods, Channel 3	Setup/Hold Time	5.0/-2.0 ns	Clk 1 ↕ Clk 2 ↕ Clk 3 ↕ Clk 4 ↕	_____ _____ _____ _____
	Setup/Hold Time	-1.5/4.5 ns	Clk 1 ↕ Clk 2 ↕ Clk 3 ↕ Clk 4 ↕	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	5.0/-2.0 ns	Clk 1 ↕ Clk 2 ↕ Clk 3 ↕ Clk 4 ↕	_____ _____ _____ _____
	Setup/Hold Time	-1.5/4.5 ns	Clk 1 ↕ Clk 2 ↕ Clk 3 ↕ Clk 4 ↕	_____ _____ _____ _____
Time Interval Accuracy		Expected	Limits	Measured
		40.96 µs	40.95571 µs to 40.96429 µs	_____

4

Calibrating and Adjusting

This chapter gives you instructions for calibrating and adjusting the logic analyzer.

Logic analyzer calibration

The logic analyzer circuitry of the Agilent 1680/90-series logic analyzers does not require an operational accuracy calibration. To test the logic analyzer circuitry against specifications (full calibration), refer to chapter 3, "Testing Performance."

5

Troubleshooting

This chapter helps you troubleshoot the logic analyzer to find defective assemblies.

The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests.

The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

NOTE: If any peripheral hardware or software programs were installed by the user into an Agilent 1680A,AD-series logic analyzer, they must be first uninstalled and removed before doing any troubleshooting. Removing user-installed hardware or software will rule out the possibility they are causing problems and/or conflicts in the logic analyzer operating system or application software. Troubleshooting is best done if the instrument is returned to its hardware and software factory configuration.

To install the fan guard

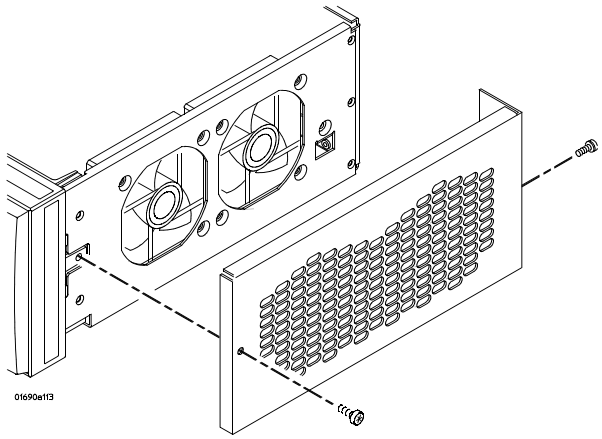
Installing the fan guard is recommended for any power-on troubleshooting for either the Agilent 1680A,AD-series or 1690A,AD-series.

NOTE: The fan guard protects repair personnel from potential injury caused by rotating fan blades.

1. Remove the chassis from the sleeve. Follow the procedure “To remove the chassis from the sleeve” on page 114 .
2. Install the fan guard onto the chassis.
   - **a** Position the chassis so the handle side is up.
   - **b** Slide the fan guard onto the chassis over the fans.

   On an Agilent 1680A,AD-series, a guide hole in the fan guard will slide over the standoff post of the bottom left rear foot (adjacent to the acquisition board BNC connectors).

c Install the optional screws as shown.

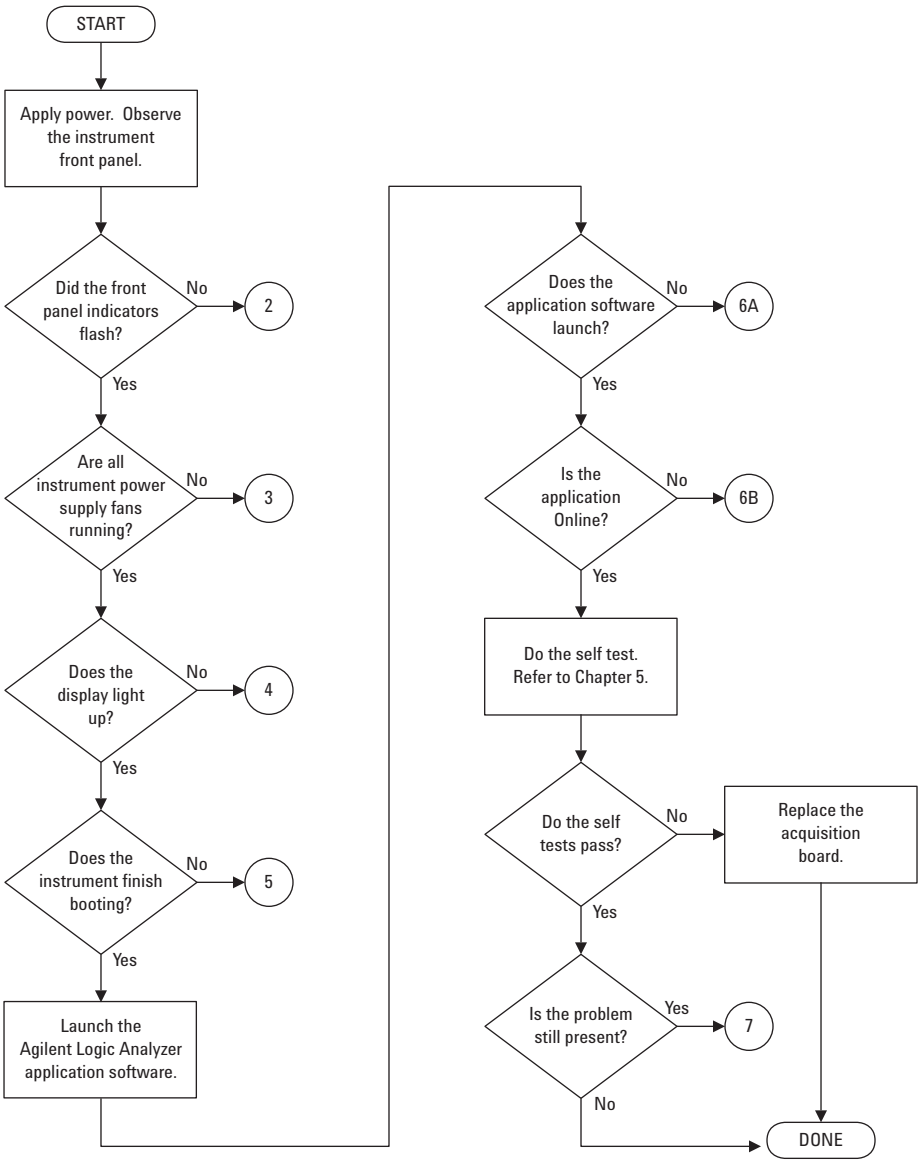


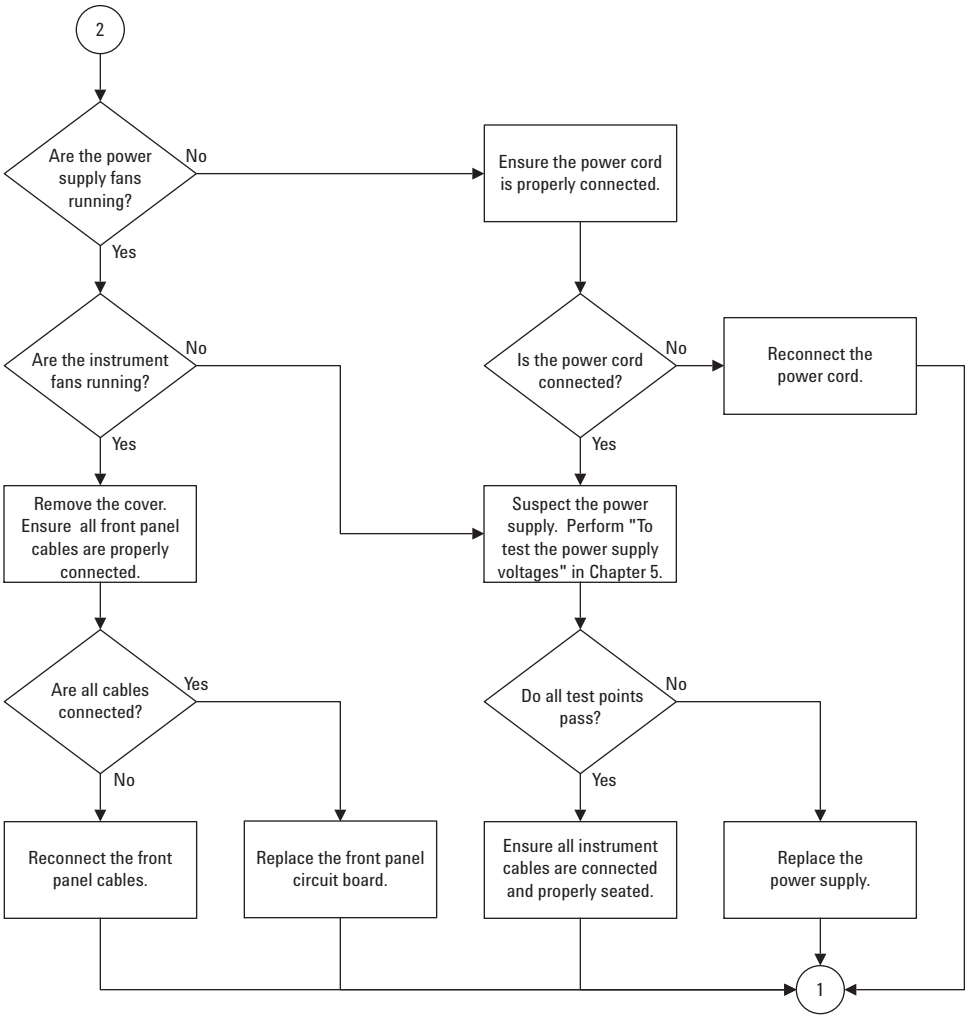
3 After the required power-on troubleshooting and repair is complete, reverse the above procedure to remove the fan guard and reassemble the instrument.

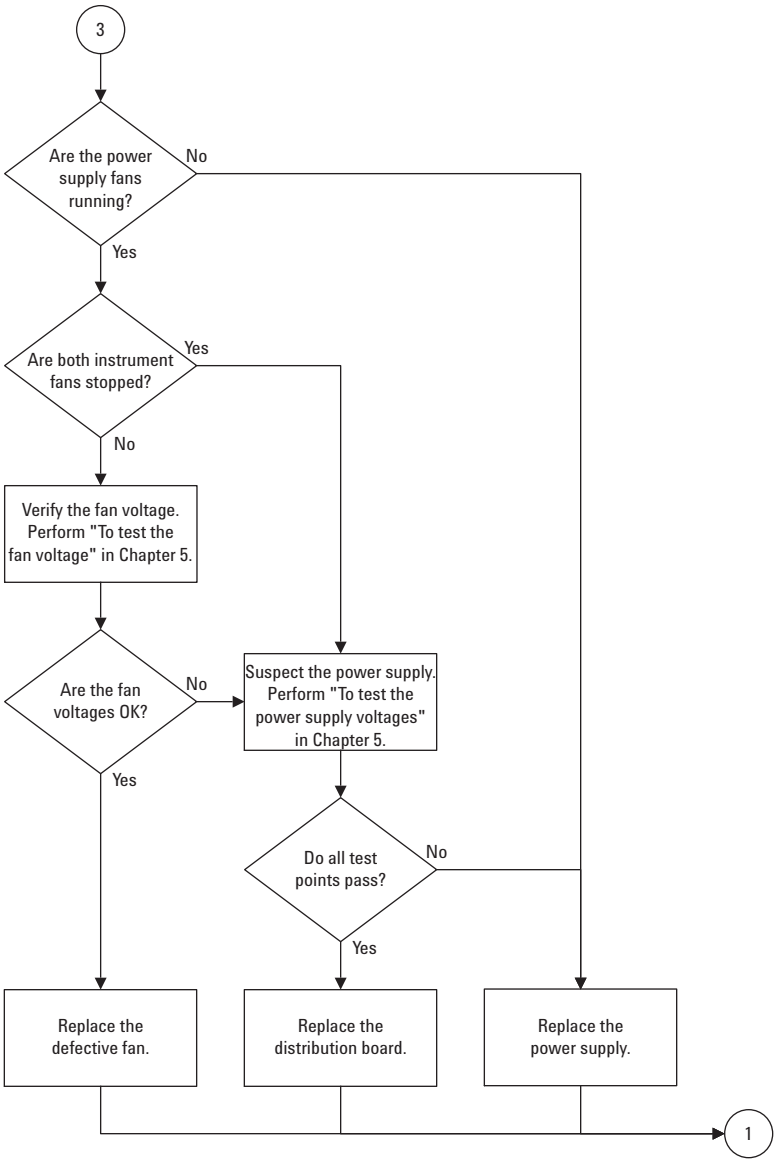
To use the flowcharts

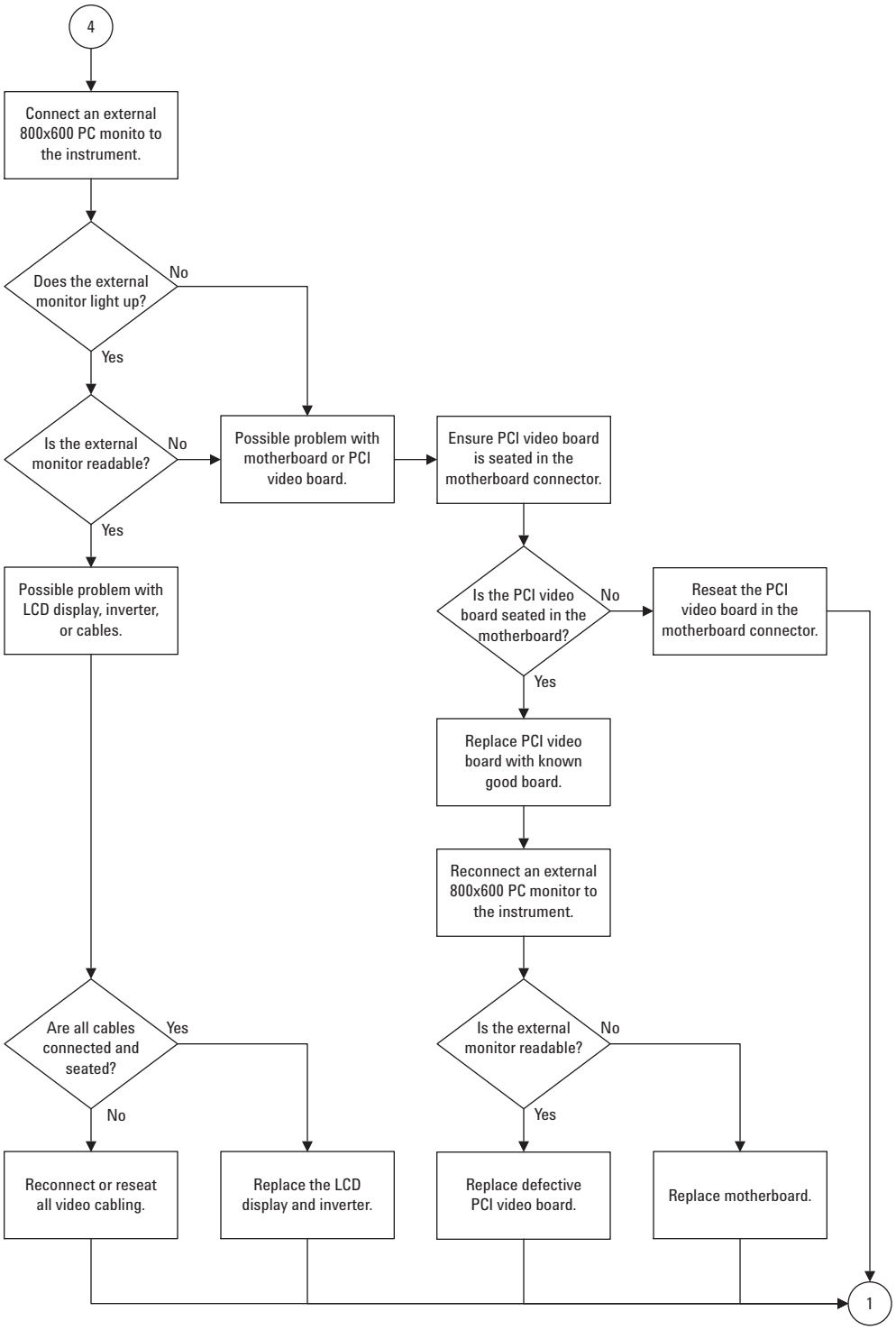
Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

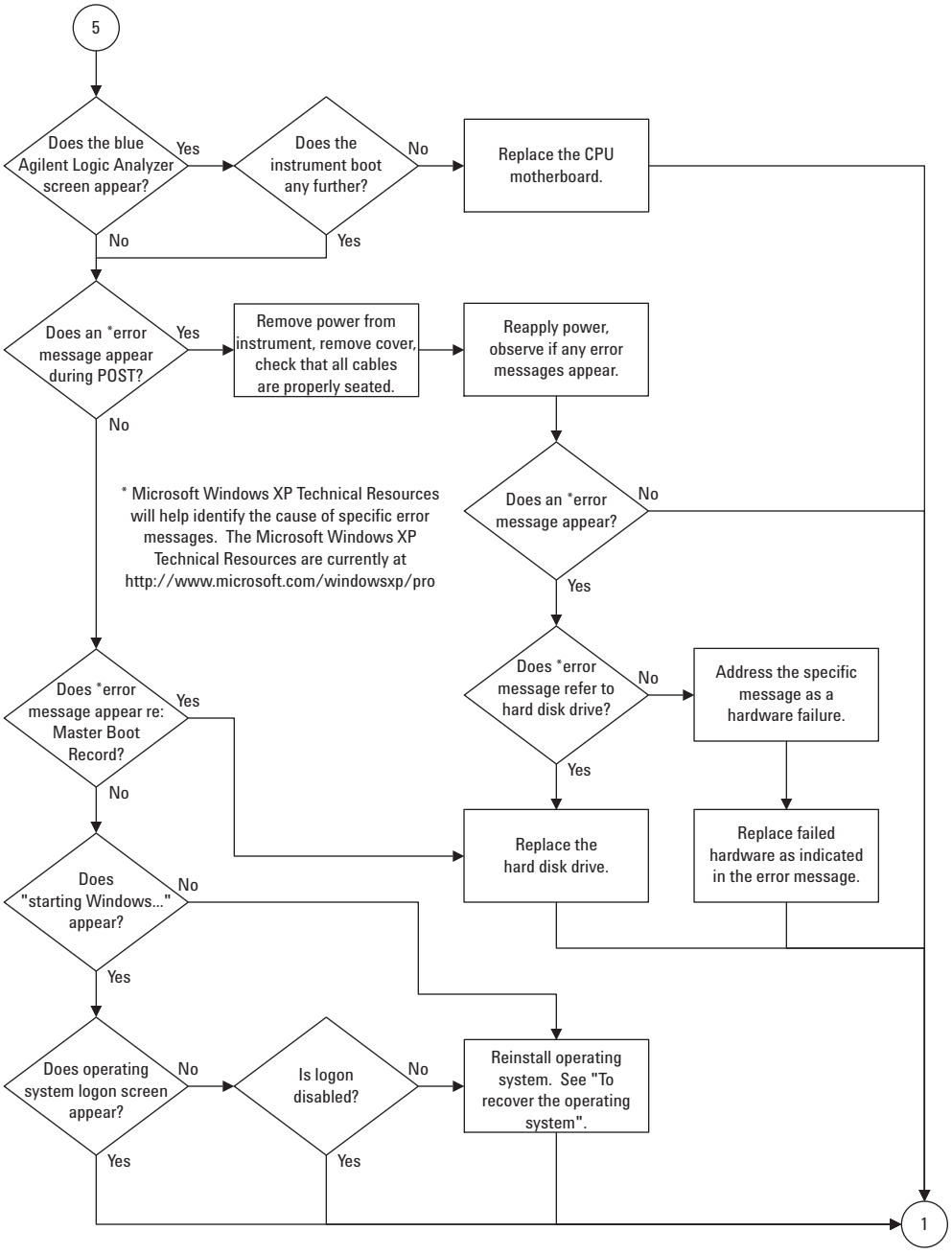
Troubleshooting the Agilent 1680A,AD-series

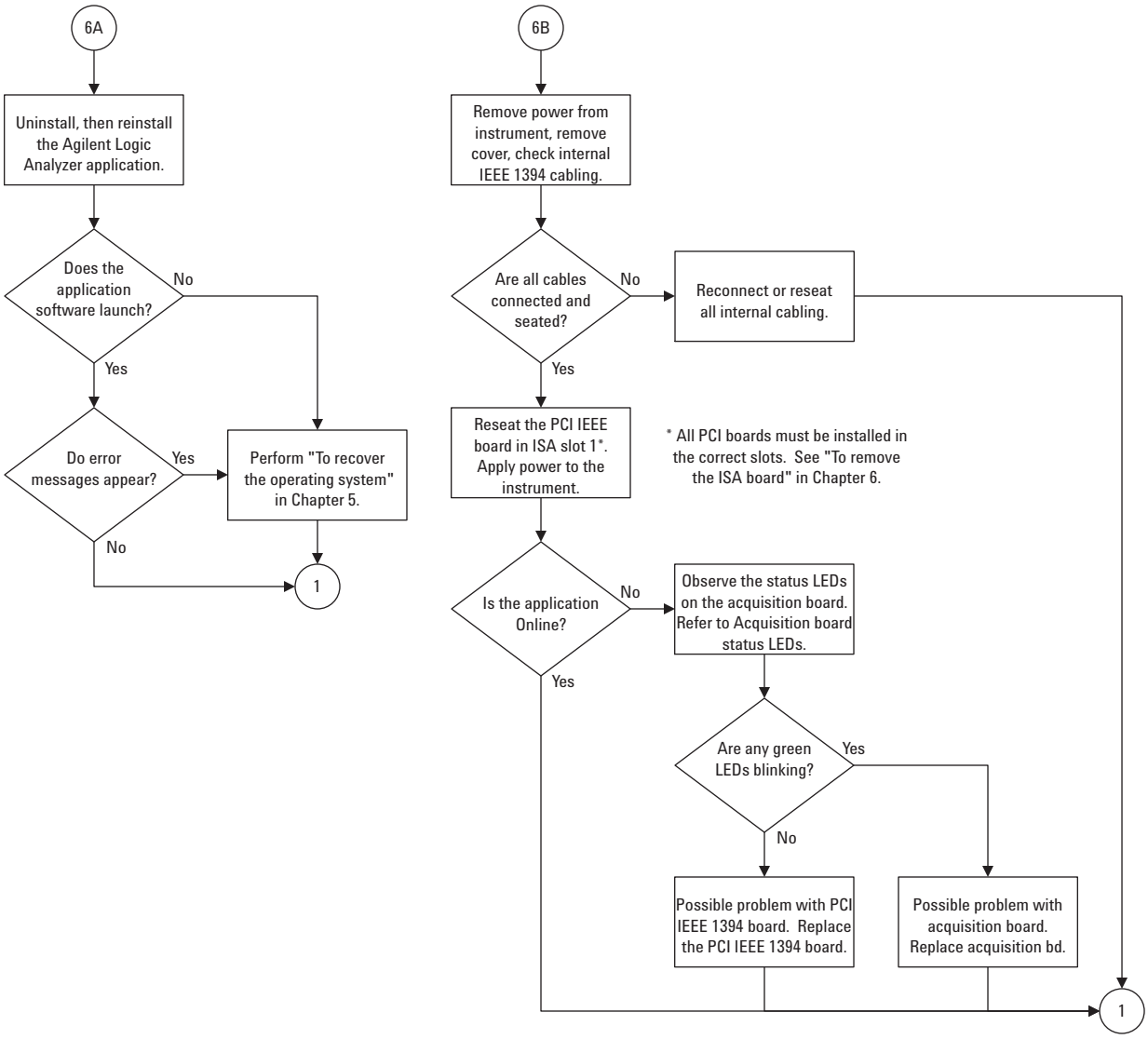


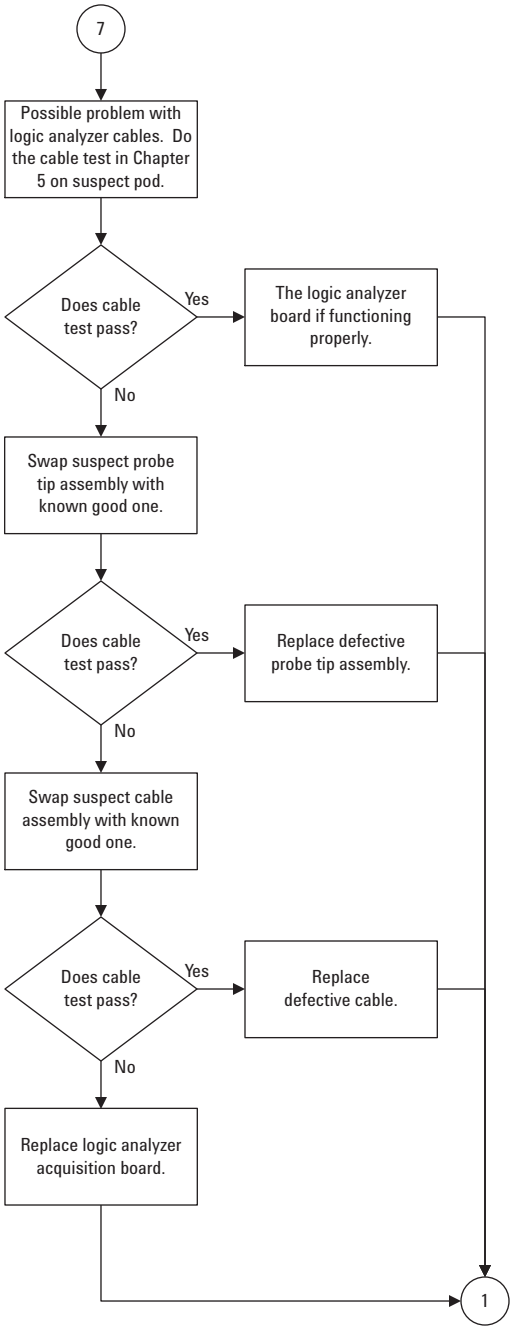

2
Are the power supply fans running?
No
Ensure the power cord is properly connected.
Yes
Are the instrument fans running?
No
Is the power cord connected?
No
Reconnect the power cord.
Yes
Yes
Remove the cover. Ensure all front panel cables are properly connected.
Suspect the power supply. Perform "To test the power supply voltages" in Chapter 5.
Are all cables connected?
Yes
Do all test points pass?
No
No
Yes
Reconnect the front panel cables.
Replace the front panel circuit board.
Ensure all instrument cables are connected and properly seated.
Replace the power supply.
1


3
Are the power supply fans running?
No
Yes
Are both instrument fans stopped?
Yes
No
Verify the fan voltage. Perform "To test the fan voltage" in Chapter 5.
Are the fan voltages OK?
No
Suspect the power supply. Perform "To test the power supply voltages" in Chapter 5.
Yes
Do all test points pass?
No
Yes
Replace the defective fan.
Replace the distribution board.
Replace the power supply.
1


4
Connect an external 800x600 PC monito to the instrument.
Does the external monitor light up?
No
Yes
Is the external monitor readable?
No
Yes
Possible problem with motherboard or PCI video board.
Ensure PCI video board is seated in the motherboard connector.
Possible problem with LCD display, inverter, or cables.
Is the PCI video board seated in the motherboard?
No
Yes
Reseat the PCI video board in the motherboard connector.
Replace PCI video board with known good board.
Reconnect an external 800x600 PC monitor to the instrument.
Are all cables connected and seated?
Yes
No
Is the external monitor readable?
No
Yes
Reconnect or reseat all video cabling.
Replace the LCD display and inverter.
Replace defective PCI video board.
Replace motherboard.
1


5
Does the blue Agilent Logic Analyzer screen appear?
Yes
Does the instrument boot any further?
No
Replace the CPU motherboard.
No
Yes
Does an *error message appear during POST?
Yes
Remove power from instrument, remove cover, check that all cables are properly seated.
Reapply power, observe if any error messages appear.
No
* Microsoft Windows XP Technical Resources will help identify the cause of specific error messages. The Microsoft Windows XP Technical Resources are currently at http://www.microsoft.com/windowsxp/pro
Does an *error message appear?
No
Yes
Does *error message refer to hard disk drive?
No
Address the specific message as a hardware failure.
Yes
Does *error message appear re: Master Boot Record?
Yes
No
Replace the hard disk drive.
Replace failed hardware as indicated in the error message.
Does "starting Windows..." appear?
No
Yes
Does operating system logon screen appear?
No
Is logon disabled?
No
Reinstall operating system. See "To recover the operating system".
Yes
Yes
1


6A
Uninstall, then reinstall the Agilent Logic Analyzer application.
Does the application software launch?
No
Yes
Do error messages appear?
Yes
Perform "To recover the operating system" in Chapter 5.
No
1
6B
Remove power from instrument, remove cover, check internal IEEE 1394 cabling.
Are all cables connected and seated?
No
Reconnect or reseat all internal cabling.
Yes
Reseat the PCI IEEE board in ISA slot 1*. Apply power to the instrument.
* All PCI boards must be installed in the correct slots. See "To remove the ISA board" in Chapter 6.
Is the application Online?
No
Observe the status LEDs on the acquisition board. Refer to Acquisition board status LEDs.
Yes
Are any green LEDs blinking?
Yes
No
Possible problem with PCI IEEE 1394 board. Replace the PCI IEEE 1394 board.
Possible problem with acquisition board. Replace acquisition bd.
1


7
Possible problem with logic analyzer cables. Do the cable test in Chapter 5 on suspect pod.
Does cable test pass?
Yes
The logic analyzer board if functioning properly.
No
Swap suspect probe tip assembly with known good one.
Does cable test pass?
Yes
Replace defective probe tip assembly.
No
Swap suspect cable assembly with known good one.
Does cable test pass?
Yes
Replace defective cable.
No
Replace logic analyzer acquisition board.
1

To check the power-up tests

The power-up self tests on the 1680A,AD-series logic analyzers is performed by the Microsoft Windows XP Professional operating system. As part of the Windows XP Professional power on self test (POST), the presence of all required system components is verified.

1. Close the Agilent Logic Analyzer application and all other applications running on the logic analyzer.
2. Shut down the instrument.
   a. Click on the Start button in the task bar, then select Shut Down.
   b. In the Shut Down window, select Shut Down from the menu, then select the OK button.
   c. After the instrument turns off, press the power button to again apply power.

Monitor the boot dialogue. When the text "Starting Windows . . ." appears at the bottom of the screen, this means required system components have been detected and have passed their power-up self-tests.

To test the power supply voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

This procedure will not expose any problems related to load regulation; however, it will show most failure modes to over 95% confidence,

WARNING: **Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.**

1. Close the Agilent Logic Analyzer application and all other applications running on the logic analyzer.
2. Shut down the instrument.
   a. Click on the Start button in the task bar, then select Shut Down.
   b. In the Shut Down window, select Shut Down from the menu, then select the OK button.

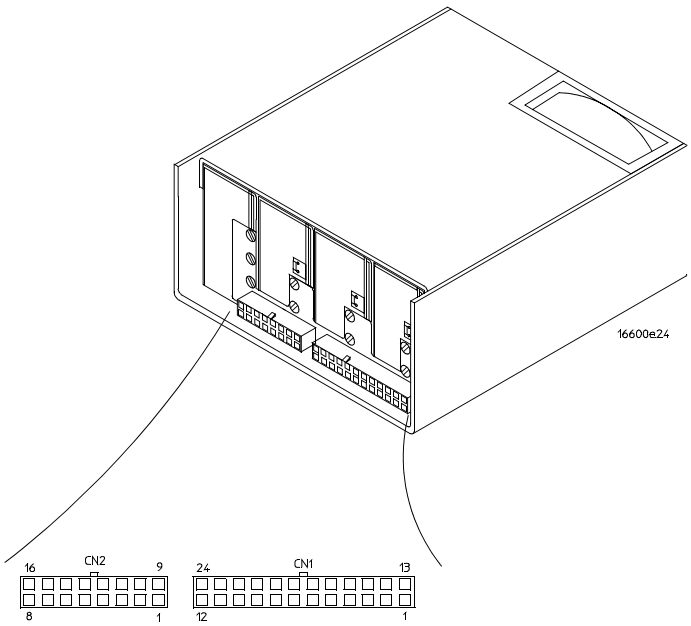
3 Remove the power supply from the instrument. Refer to “To remove the power supply” in Chapter 6.

4 After removing the power supply, connect a power cord to the power supply and plug the power cord into line power.

5 Using DVM, measure the power supply voltages.

Power Supply Voltages

CN1		CN2	
Pin	**Voltage**	**Pin**	**Voltage**
1-5	+3.3 V	1-4	-5.2 V
6-7	COM	5	+12 V
8-10	+5 V	6-8	-12 V
11-12	COM	9-12	COM
13-14	+3.3 V	13	+12 V
15-19	COM	14-16	COM
20-21	+5 V		
22-24	COM		



6 Note problems with the power supply, then unplug the power supply from line power. Return to the flow chart.

To test the LCD display signals

Before attempting to do this procedure, ensure that the video signal cable connected to the PCI video board is properly seated. Attempt to reseat the cable two or three times. If other repairs were done to the instrument, and the video is now no longer operating, it is very likely that the video cable is not properly seated.

Refer to chapter 6, "Replacing Assemblies", for instructions to remove or replace covers and assemblies.

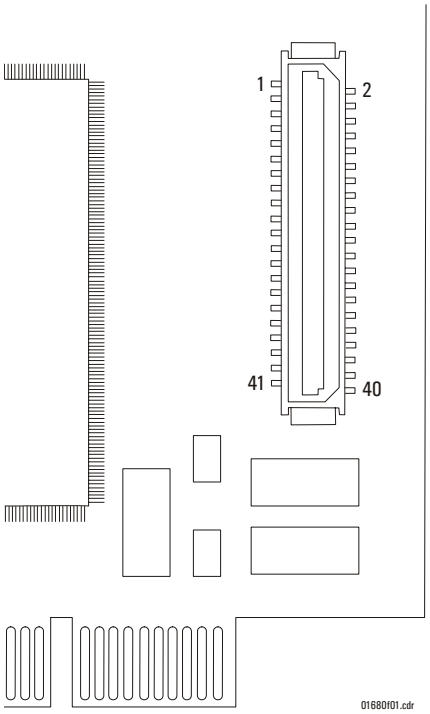
WARNING: **Warning Hazardous voltages exist on the power supply and the LCD display, and the LCD inverter. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electric shock.**

1. Remove the sleeve. Refer to chapter 6 for more information on how to remove the sleeve.
2. Connect a power cord to the instrument and apply power.
3. Using an oscilloscope, probe the following pins of J111 for digital signals.

   2, 4, 5

   9, 10, 11, 13, 14, 15

   29, 30, 31, 33, 34, 35, 37



4 Using an oscilloscope, probe pins 39 and 40 of J111 for +3.3Vdc

If +3.3Vdc is present on J111 of pins 39 and 40, and digital signals are present on the video data pins indicated above, then the CPU board video circuit is operating properly.

5 Remove power. Allow time for the capacitors in the power supply to discharge before disconnecting the power supply, doing the repair, and reassembling the instrument.

To test disk drive voltages

The following procedure is a guide to help further identify possible problems with either the flexible disk drive or hard disk drive.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B

1 Close the Agilent Logic Analyzer application and all other applications running on the logic analyzer.

2 Shut down the instrument.

a Click on the Start button in the task bar, then select Shut Down.

b In the Shut Down window, select Shut Down from the menu, then select the OK button.

3 After the instrument turns off, unplug the instrument and remove the cover.

4 Disconnect the suspect disk drive. Remove the disk drive from the chassis and reconnect the cable.

5 Troubleshoot a hard disk drive.

a Apply power to the instrument.

b As the instrument is booting, probe for digital signals on the hard disk drive connector according to the following table.

Disk Drive Voltages

Pin No.	Signal	Voltage	Pin No.	Signal	Voltage	Pin No.	Signal	Voltage
1	RESET		27	IORDY		34	PDIAG	
3 - 18	DATA		28	CSEL		35	DA00	
20	KEY		29	DMACK		36	DA02	
21	DMARQ		31	INTRQ		37	CS0	
23	DIOW		32	IOCS16		38	CS1	
25	DIOR		33	DA01		39	DASP	

Pins 2, 19, 22, 24, 26, 30, 40, are GROUND
Pins 41 and 42 are +5 Vdc

6 Troubleshoot a flexible disk drive.

a Apply power to the instrument.

b After the instrument finished booting, launch the Agilent Logic Analyzer application.

c Insert a formatted flexible disk in the instrument flexible disk drive.

d Attempt to do a File Save of the Agilent Logic Analyzer default configuration to the flexible disk drive.

e While the instrument is attempting to save the file to flexible disk, probe for digital signals on the flexible disk drive connector according to the following table.

Disk Drive Voltages

Pin	Signals	Pin No.	Signal
1	+5 V	2	INDEX
3	+5 V	4	DRIVE SELECT
5	+5 V	6	DISK CHANGE
7	NC	8	READY
9	NC	10	MOTOR ON
11	NC	12	DIRECTION SELECT
13	NC	14	STEP
15	0 V	16	WRITE DATA
17	0 V	18	WRITE GATE
19	0 V	20	TRACK 00
21	0 V	22	WRITE PROTECT
23	0 V	24	READ DATA
25	0 V	26	SIDE ONE SELECT

7 Repeat steps 1 through 3 above. After the instrument turns off, unplug the instrument.

8 Replace suspect disk drive if necessary, then reassemble the instrument.

To verify the CD-ROM

The CD-ROM drive itself can be tested using an audio CD. Install CD player-style headphones in the CD-ROM audio output jack. With the instrument powered on, insert an audio CD into the CD-ROM drive. If the CD-ROM is operating properly, it should begin playing the audio CD.

To recover the operating system

To reinstall the operating system

Reinstalling the operating system erases the entire hard disk drive and reinitializes the hard disk drive to its factory configuration. All user data stored on the hard disk drive will be lost. Reinstalling the operating system is necessary in case any system level files or other components of the operating system become corrupted.

The recovery CD-ROM contains an image of the Windows XP Professional operating system. The CD-ROM contains an install key which recognizes whether or not the system motherboard is an Agilent logic analyzer motherboard. If the system motherboard is an Agilent logic analyzer motherboard, then the install key permits the recovery of the operating system from the CD-ROM to the hard disk drive.

1. Apply power to the instrument.
2. After applying power, insert the recovery CD-ROM in the instrument CD-ROM drive.

   If the instrument finishes booting, then user files can likely be archived so they don't become lost.
3. Press the on/off button to turn the instrument off.
4. After a few seconds turn the instrument back on.
5. At the prompt, select "Yes" to reinstall the operating system.

   It takes about 1 hour to reinstall the operating system and Agilent Logic Analyzer application software. At the end of the operating system reinstallation, the logic analyzer will be in its factory default operating system configuration.

Problems running the Application Software

If there is a problem while running the Agilent Logic Analyzer application software, then the likely cause would be the application if the error or unusual behavior appeared while configuring a window or analyzing data.

In the event of a problem of the Agilent Logic Analyzer application software, do the following steps:

In case the application software becomes unresponsive, do a Ctrl-Alt-Del and follow the queries to abort the application software. Attempt to restart the application software and do a measurement.

If there are still problems running the application software, then uninstall and reinstall

the application software.

Problems with the Operating System

Operating system applies to the Agilent 1680A,AD-series logic analyzers. The likely cause would be the operating system if the error or unusual behavior appeared while doing an operating system task, like printing or configuring the network.

In the event of a problem with the operating system, do the following steps:

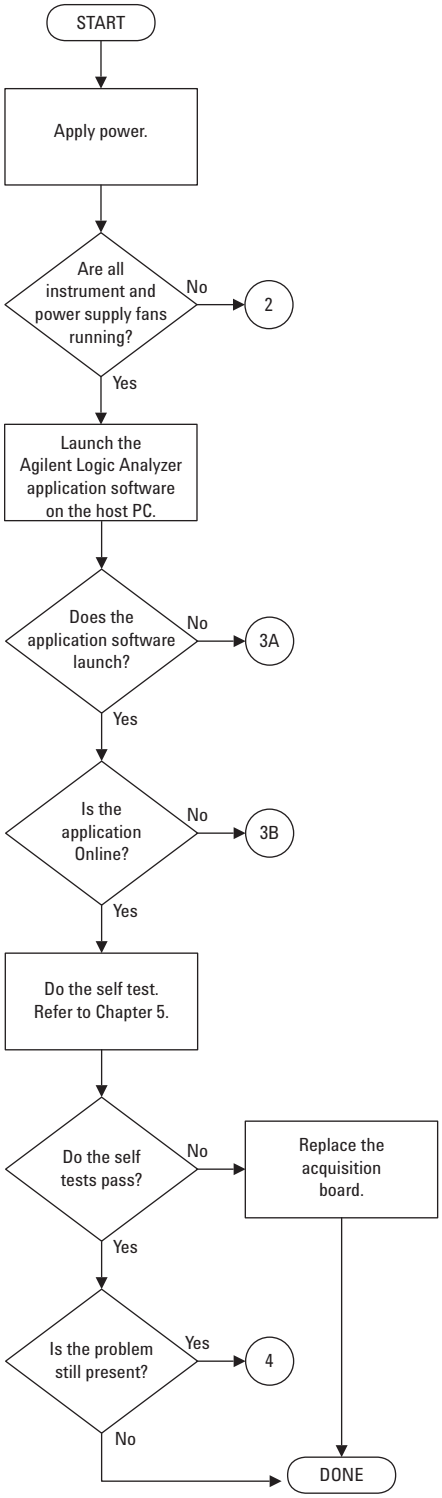
If error messages appear, consult the operating system documentation for information related to the errors.

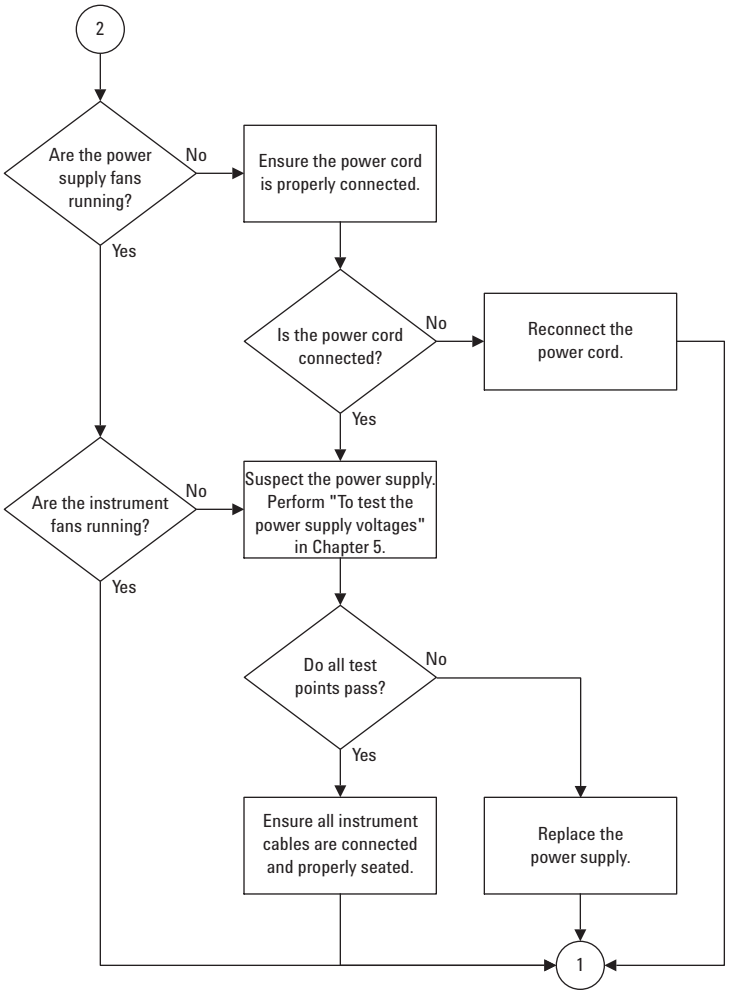
In case the whole system becomes unresponsive, turn the instrument off by pressing the on/off button. If pressing the on/off button does not initiate the power-down routine, then press and hold the on/off button for 5 seconds until the instrument turns off.

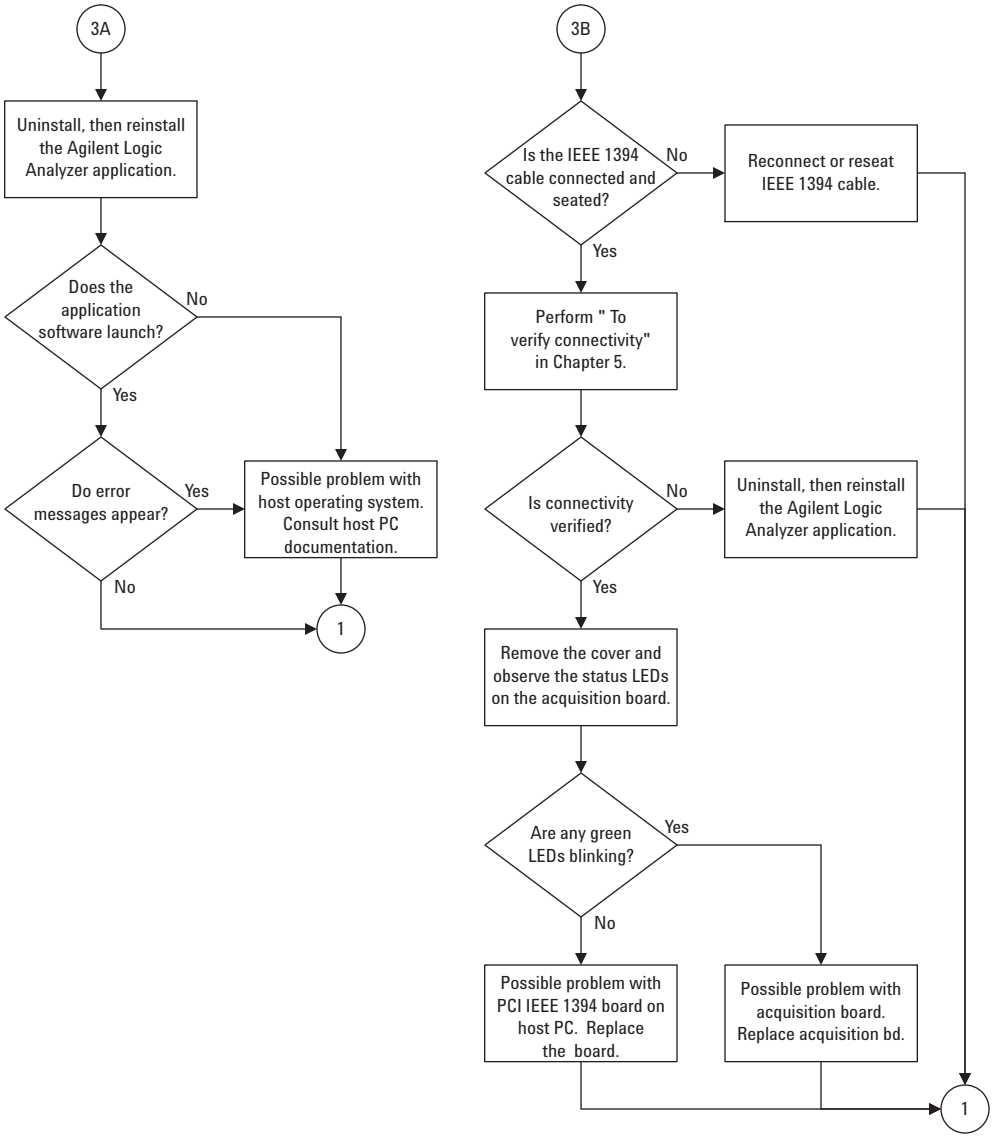
Turn on the instrument and reattempt the task. If the whole system again becomes responsive then follow the above procedure To reinstall the operating system.

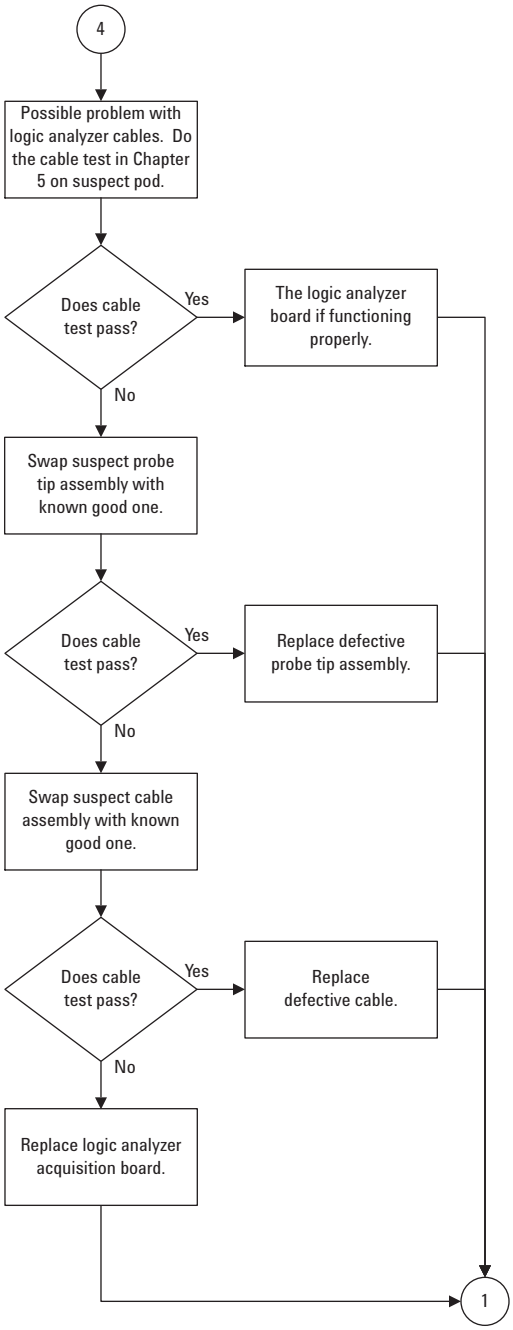
For a host PC controlling an Agilent 1690A,AD-series hosted logic analyzer, responsibility of diagnosing errors and problems with utilized system services is the user's.

Troubleshooting the Agilent 1690A,AD-series




2
Are the power supply fans running?
No
Ensure the power cord is properly connected.
Yes
Is the power cord connected?
No
Reconnect the power cord.
Yes
Are the instrument fans running?
No
Suspect the power supply. Perform "To test the power supply voltages" in Chapter 5.
Yes
Do all test points pass?
No
Yes
Ensure all instrument cables are connected and properly seated.
Replace the power supply.
1


3A
Uninstall, then reinstall the Agilent Logic Analyzer application.
Does the application software launch?
No
Yes
Do error messages appear?
Yes
Possible problem with host operating system. Consult host PC documentation.
No
1
3B
Is the IEEE 1394 cable connected and seated?
No
Reconnect or reseat IEEE 1394 cable.
Yes
Perform " To verify connectivity" in Chapter 5.
Is connectivity verified?
No
Uninstall, then reinstall the Agilent Logic Analyzer application.
Yes
Remove the cover and observe the status LEDs on the acquisition board.
Are any green LEDs blinking?
Yes
No
Possible problem with PCI IEEE 1394 board on host PC. Replace the board.
Possible problem with acquisition board. Replace acquisition bd.
1

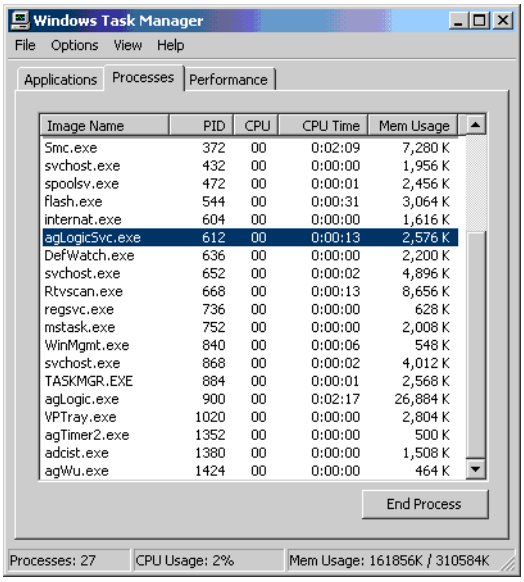

4
Possible problem with logic analyzer cables. Do the cable test in Chapter 5 on suspect pod.
Does cable test pass?
Yes
The logic analyzer board if functioning properly.
No
Swap suspect probe tip assembly with known good one.
Does cable test pass?
Yes
Replace defective probe tip assembly.
No
Swap suspect cable assembly with known good one.
Does cable test pass?
Yes
Replace defective cable.
No
Replace logic analyzer acquisition board.
1

To verify connectivity

Using Windows Device Manager and Task Manager, you can quickly determine if the Agilent Logic Analyzer application software is correctly installed on a host PC.

Task Manager

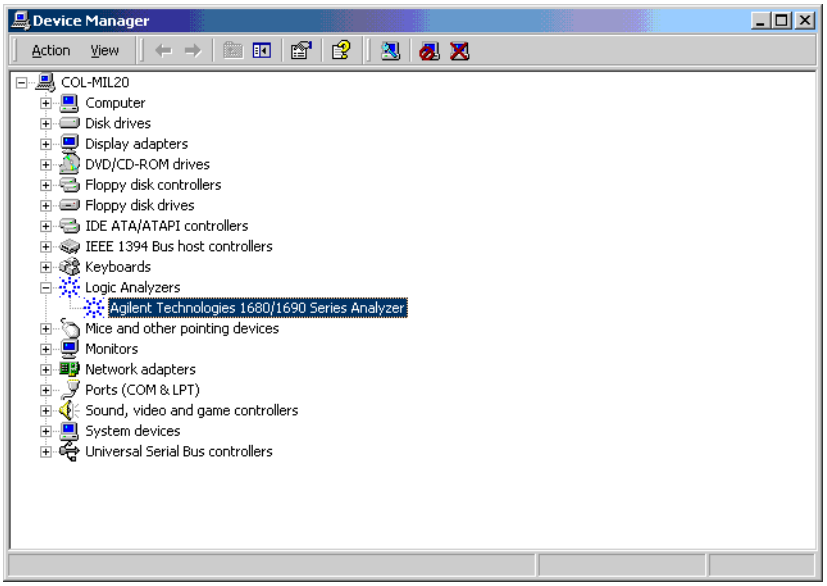
Use Task Manager to see if the agLogicSvc is running. The agLogicSvc is started when the PC is booted and establishes connection with the 1690A,AD-series hosted logic analyzer when the logic analyzer is connected to the PC. If the agLogicSvc service is not listed, then the host PC will not be able to establish an interface with the hosted logic analyzer.



If the agLogicSvc service is not listed, then uninstall and reinstall the Agilent Logic Analyzer application software. If the agLogicSvc service still does not appear, then there is a problem with your Windows XP Professional operating system. Consult the documentation for the operating system to further determine why the service is not being installed and run.

Device Manager

Use Device Manager to see if the Agilent Logic Analyzer device has been properly installed. The Device Manager should include an entry "Logic Analyzers" with the device "Agilent Technologies 1680/1690 Series Analyzer".



If the logic analyzer device is not listed, then uninstall and reinstall the Agilent Logic Analyzer application software. If the device still does not appear, then there is a problem with the Windows XP Professional operating system. Consult the documentation for the operating system to determine why the device is not being installed and run.

To test the power supply voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

This procedure will not expose any problems related to load regulation; however, it will show most failure modes to over 95% confidence,

WARNING: **Hazardous voltages exist on the power supply. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.**

1 Close the Agilent Logic Analyzer application and all other applications running on the logic analyzer.

2 Shut down the instrument.

a Click on the Start button in the task bar, then select Shut Down.

b In the Shut Down window, select Shut Down from the menu, then select the OK button.

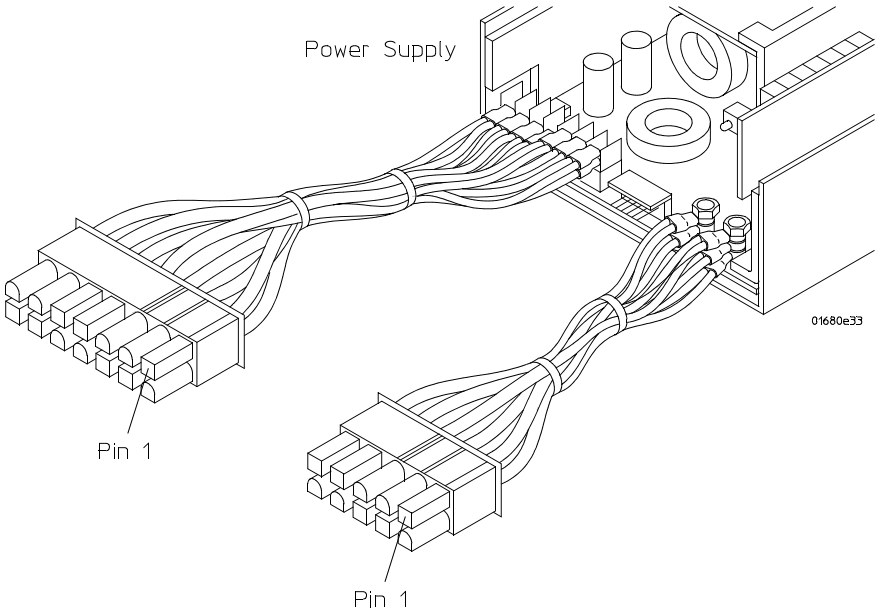
3 Remove the power supply from the instrument. Refer to "To remove the power supply" in Chapter 6.

4 After removing the poser supply, connect a power cord to the power supply and plug the power cord into line power.

5 Using DVM, measure the power supply voltages.

Power Supply Voltages

CN1		CN2	
Pin	**Voltage**	**Pin**	**Voltage**
1-3	+3.4 V	1,2	+5.1 V
4,5	COM	3	COM
6,7	+3.4 V	4	-5.2 V
8-10	COM	5,6	COM
		7	+12 V
		8	+5.1 V
		9,10	COM
		11,12	-5.2 V
		13	COM
		14	+12 V



6 Note problems with the power supply, then unplug the power supply from line power. Return to flow chart.

General Troubleshooting

This section includes troubleshooting procedures that can be done on either the Agilent 1680A,AD- or 1690A,AD-series logic analyzers. Before any of these procedures can be done on an Agilent 1690A,AD-series logic analyzer, the logic analyzer must be connected to a host PC and both the host PC and the logic analyzer must be turned on.

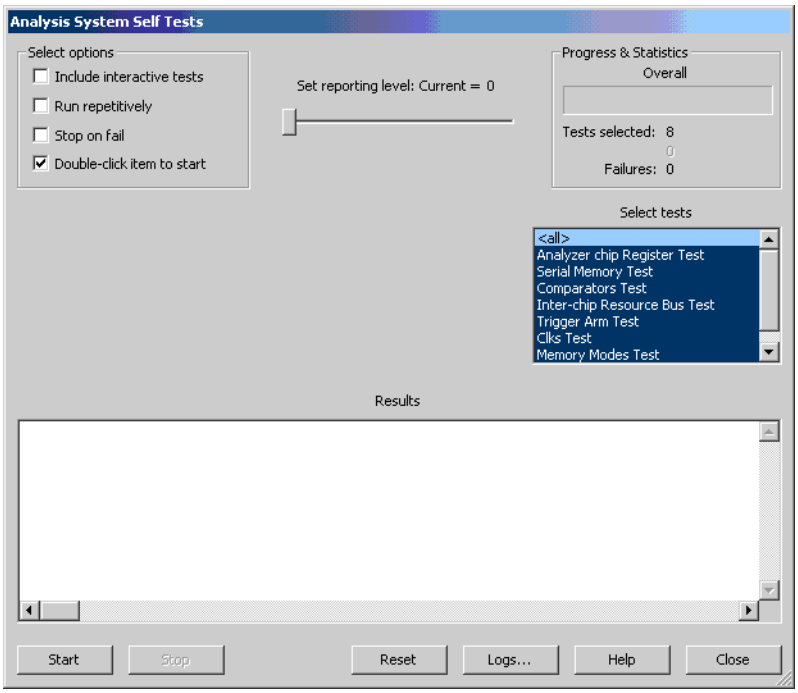
To run the self-tests

The Self Test menu checks the major hardware functions of the logic analyzer to verify that it is working correctly. Self-tests can be performed all at once or one at a time. Refer to Chapter 8 for more information on the logic analyzer self-tests.

CAUTION: Because the most recently acquired data will be lost, be sure to save important data before running self tests.

1. Do the following steps for an Agilent 1690A,AD-series:
   - **a** Connect the logic analyzer to a host PC and apply power.
   - **b** Apply power to the host PC and allow the PC to finish booting.
2. For an Agilent 1680A,AD-series logic analyzer, apply power to the instrument and allow it to finish booting.
3. Launch the Agilent Logic Analyzer application. When the application launches, observe the status field and ensure it reads “Online.”
4. In the Agilent Logic Analyzer application, choose Help>Self Test... from the main menu.

CAUTION: If you have acquired data, a warning message appears, "Running self-tests will invalidate acquired data"; click OK to continue.



5 In the Analysis System Self Tests dialog, select the self test options:

- Include interactive tests — causes interactive tests to appear in the selection lists.
- Run repetitively — runs the selected tests repetitively until you click Stop.
- Stop on fail — if you are running multiple tests or running tests repetitively, this causes the tests to stop if there is a failure.
- Double-click item to start — lets you double-click a test to start it.

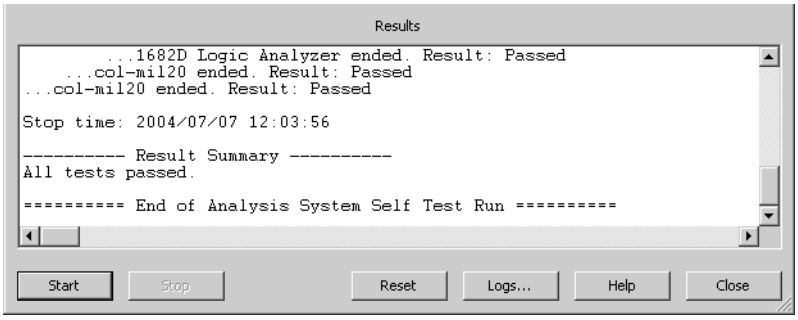
6 Set the reporting level.

Higher levels produce increasingly verbose output.

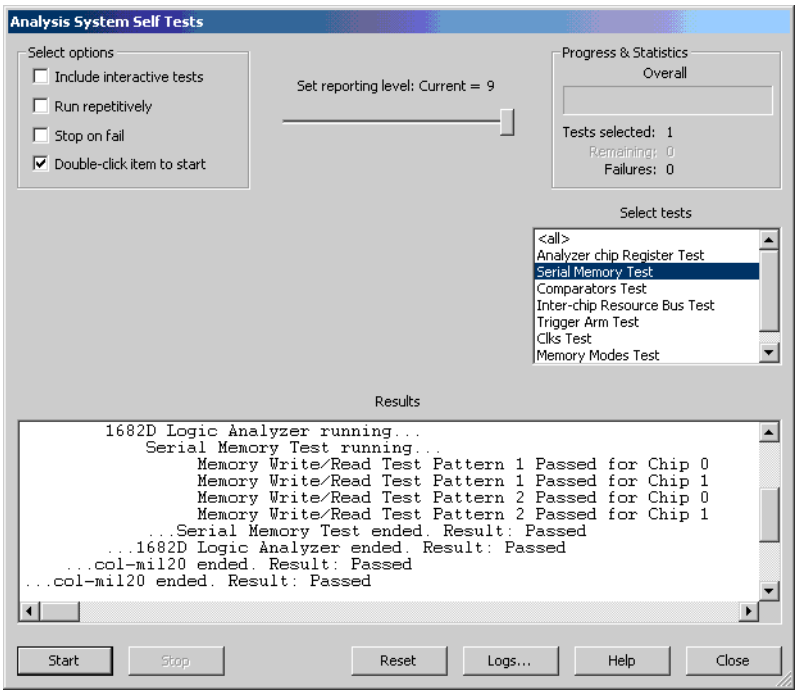
7 Select the tests you want to run.

8 Click Start.

As the tests are running, the results are reported in the lower part of the dialog and saved to a log file.



The self tests can be run one at a time by clicking on the self-test of interest. The results of the individual test will be reported under Results. For example, if you select the Serial Memory Test and the highest reporting level, the following results should be reported in the status window:



To stop a running test, click Stop.

To reset the self-test options, click Reset.

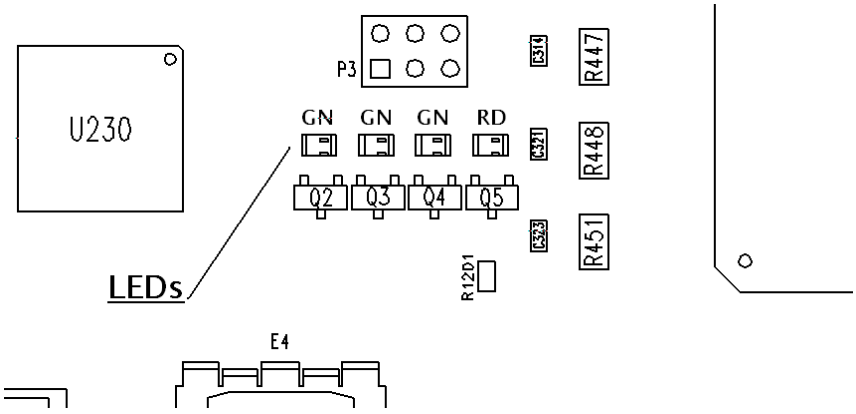
To view the log file, click Logs..., select the log file you want to view, and click Open.

If, after completing the self tests, you have failures or you have questions about the performance of the logic analysis system, contact Agilent Technologies sales or support at http://www.agilent.com/find/contactus.

9 Click Close to close the Analysis System Self Tests dialog.

Acquisition board status LEDs

The acquisition board has four LEDs located close to its IEEE 1394 port. The LEDs report the status of configuration of both the interface field programmable gate array (FPGA) and the IEEE 1394 link layer on the acquisition board.



Green LEDs

The green LEDs display the status of loading of the IEEE 1394 link layer.

When the IEEE 1394 is successfully loaded, the system processor on the CPU Motherboard can communicate with the acquisition board. The system processor can then configure and download information from the acquisition board.

Red LED

The Red LED shows the status of the configuration software load of the interface FPGA in the acquisition board.

When the Red LED is on and steady, this indicates the FPGA configuration software has not been successfully loaded into the FPGA. Failure to load the FPGA configuration can be caused by either a failure of the acquisition board or a failure of the PCI IEEE 1394 board. Failure to load the FPGA configuration can also be caused by a missing or misconfigured agLogicSvc service.

Normal Operation

During normal operation, the red LED is off and all three green LEDs are illuminated.

During power up (1680A,AD-series) or connection (1690A,AD-series), the green LEDs first blink on then off. The acquisition board processor attempts to initialize and load the IEEE 1394 link layer. The individual status LEDs represent the success or failure of three steps needed to initalize, load, and then run the IEEE 1394 link layer. When each of the green LEDs illuminate:

LED #1 (closest to the red LED) - the on-board processor is properly initialized and running, attempting to load the IEEE 1394 link layer configuration

LED #2 - the IEEE 1394 link layer is loaded and configured

LED #3 - the IEEE 1394 is loaded, properly configured, and is running

A blinking green LED signifies a failure of one of the above steps. In this case, the acquisition board must be replaced.

When the IEEE 1394 port on the acquisition board is configured and initialized, the agLogicSvc service running on the Windows XP Professional operating system senses the acquisition board. The agLogicSvc service then loads configuration code into the interface FPGA on the acquisition board. When the FPGA is configured, the red LED is turned off. The acquisition board is then properly configured and initialized both to communicate with the system processor and to acquire data.

To test the logic analyzer probe cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	200 MHz, 2.5 ns pulse width, < 600 ps rise time	8133A Option 003
Adapter (Qty 4)	SMA (m) - BNC (f)	1250-1200
Coupler (Qty 4)	BNC (m)(m)	1250-0216
6x2 Test Connectors (Qty 4)		

1 Turn on the equipment and the logic analyzer.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Trigger	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide 1	Mode: Square
Period: 20.000 ns	Divide: Square ÷ 1	Ampl: 0.50 V	Delay: 0.000 ns
		Offs: 0.00 V	
	Ampl: 0.80 V		Ampl: 0.80 V
	Offs: -1.30 V		Offs: -1.30 V
	COMP: Disabled (LED Off)		COMP: Disabled (LED Off)

3 Using four 6-by-2 test connectors, four BNC Couplers, and four SMA (m) - BNC (f) Adapters, connect the logic analyzer to the pulse generator channel outputs (to make the test connectors, see chapter 3, "Testing Performance"):

a Connect the even-numbered channels of the lower byte of the pod under test and Clk 1 to the pulse generator channel 1 OUTPUT.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{OUTPUT}}$.

c Connect the even-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 OUTPUT.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 $\overline{\text{OUTPUT}}$.

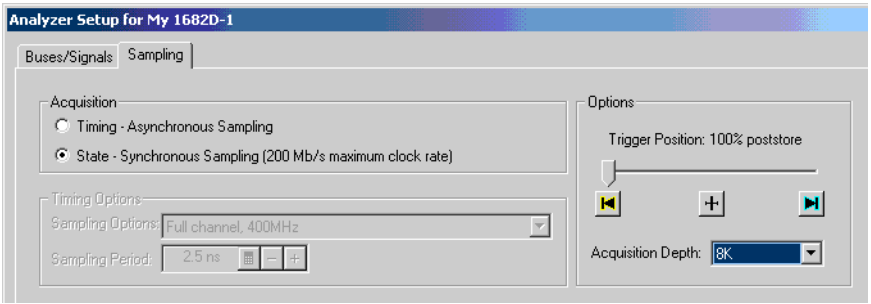
4 Configure the Analyzer Setup dialog:

a In the Waveform window, click on the Sampling Setup icon.

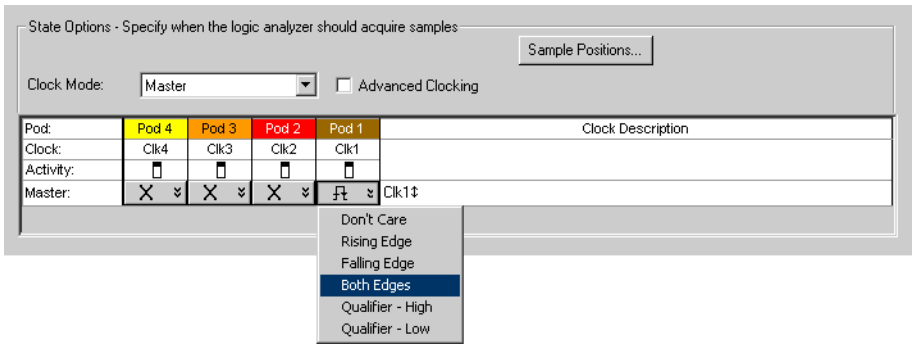
b In the Analyzer Setup dialog, select State - Synchronous Sampling.

c Configure Trigger Position - 100% poststore.

d Select an Acquisition Depth of 8K.



e Click the Master button for the clock to be tested; then, select Both Edges.

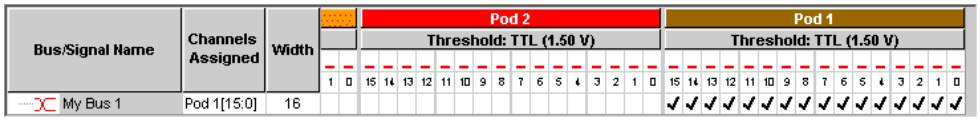


5 Configure the pod under test:

a In the Analyzer Setup dialog, click the Buses/Signals tab

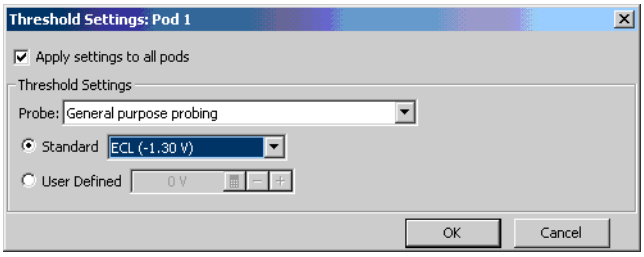
b Click Delete All at the bottom of the window.

c Using the mouse, activate all channels for the pod under test. Assign channels to bus/signal name My Bus 1.



d Click on the threshold field for the pod under test. The Threshold Settings dialog appears.

e In the Threshold Settings dialog, select Standard and ECL (-1.30 V).



f Click OK to close the the Threshold Settings dialog.

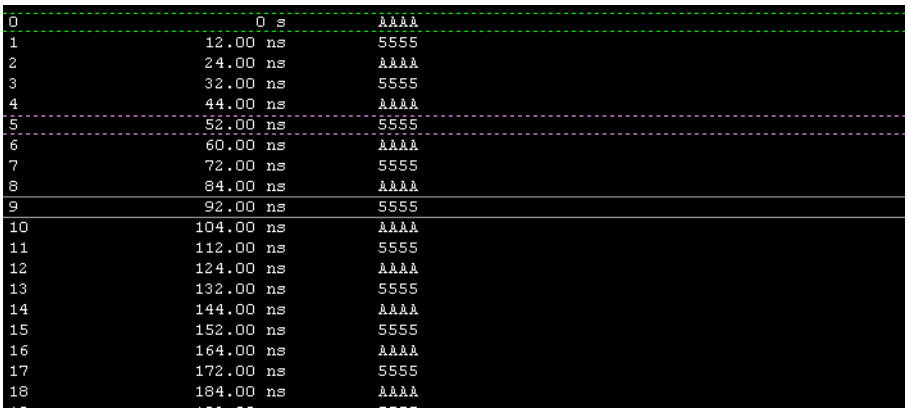
g Click OK to close the Analyzer Setup dialog.

6 Verify the data:

a Click the Listing - Listing 1 tab.

b In the Listing window, click the Run icon. The display should look

similar to the figure below.



0	0 s	AAAA
1	12.00 ns	5555
2	24.00 ns	AAAA
3	32.00 ns	5555
4	44.00 ns	AAAA
5	52.00 ns	5555
6	60.00 ns	AAAA
7	72.00 ns	5555
8	84.00 ns	AAAA
9	92.00 ns	5555
10	104.00 ns	AAAA
11	112.00 ns	5555
12	124.00 ns	AAAA
13	132.00 ns	5555
14	144.00 ns	AAAA
15	152.00 ns	5555
16	164.00 ns	AAAA
17	172.00 ns	5555
18	184.00 ns	AAAA

7 Repeat steps 3 through 7 to test other logic analyzer cables.

8 Disconnect the test equipment from the logic analyzer.

9 If the display looks like the figure, the cable passed the test.

If the display does not look similar to the figure, there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include the following:

- Open channel.
- Channel shortened to a neighboring channel.
- Channel shortened to either ground or a supply voltage.

Return to Troubleshooting flowchart 7.

To check the BNC Trigger input/output signals

1 Turn on the equipment and the logic analyzer.

2 Set up the DC source to deliver a DC voltage on the output:

a In the function generator Utility menu, activate the DC Level. All AC voltage functions will be disabled.

b Enable the high impedance load under the Output Setup menu.

3 Connect the equipment to the logic analyzer:

a On the DC source, enter a voltage setting of 0.000 V.

b Using a BNC cable, connect the output of the DC Source to the logic

analyzer Trigger In BNC.

c Using a BNC-banana cable, connect the voltmeter to the logic analyzer Trigger Out BNC.

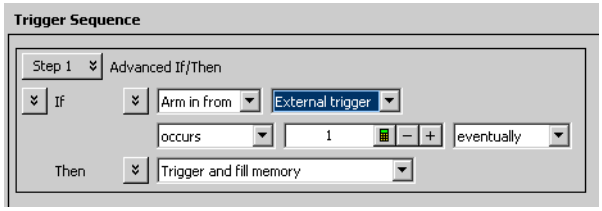
The voltmeter will display a voltage approximately 3 Vdc.

4 Configure the external trigger:

a Select the Trig Trigger Setup icon.

b In the Advanced Trigger dialog, for Trigger Sequence Step 1, select "Arm in from" instead of "Anything" as the event to trigger on.

c Then, select "External trigger" as the source of the arming signal.



d Click OK to close the Advanced Trigger dialog.

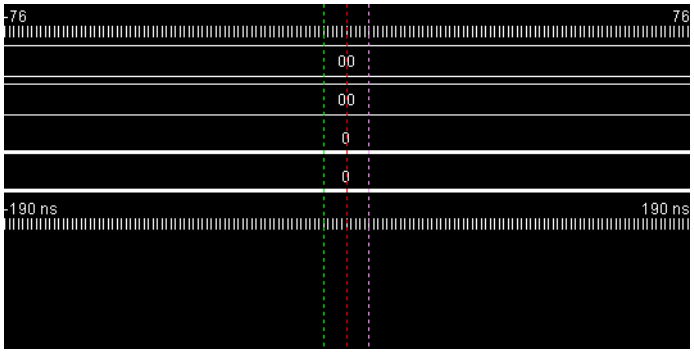
5 Verify the external trigger:

a Select the Run icon.

The logic analyzer will report "Waiting in Trigger Step 1...". The voltmeter will display approximately 0 Vdc.

b On the DC source, enter a voltage setting of 3.000 V.

The voltmeter will display approximately 3 Vdc. The logic analyzer will trigger and display a waveform similar to the following:



c On the DC source, re-enter the voltage setting of 0.000 V.

6 Disconnect the test equipment from the logic analyzer.

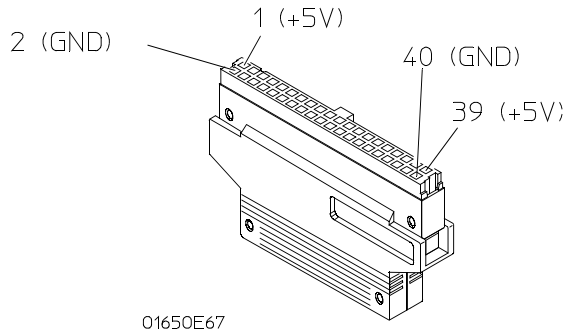
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection device. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	E2373A

- Use the multimeter to verify the +5 V on pins 1 and 39 of the probe cables.



6

Replacing Assemblies

This chapter contains the instructions for removing and replacing the assemblies of the logic analyzer. Also in this chapter are instructions for returning assemblies.

1680A,AD-series disassembly/assembly

Prepare the instrument for disassembly

Do this procedure before doing any disassembly procedure on the instrument.

1. Close the Agilent Logic Analyzer application software.
2. Gracefully shut down the operating system and remove power when shutdown is complete.
3. Remove the power cord.
4. Move the instrument to a static safe work environment.

To remove the chassis from the sleeve

Before disassembling the instrument, it must be turned off and placed in a static safe work environment. If you haven't already done so, do the previous procedure "Prepare the instrument for disassembly."

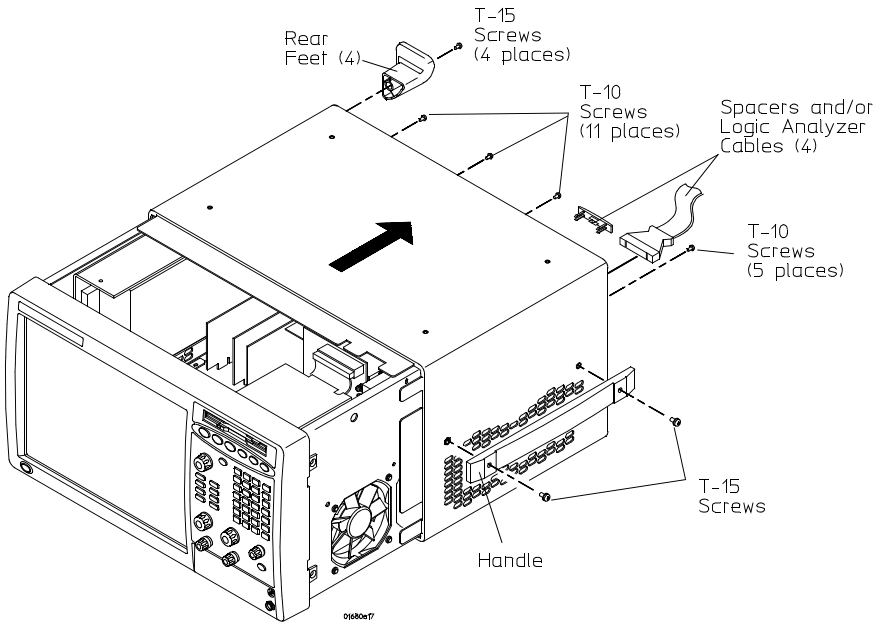
1. Using a Torx T-15 screwdriver, remove the two screws that secure the handle to the side of the instrument and lift off the handle.
2. Using a Torx T-10 screwdriver, remove five screws that secure the logic analyzer cables to the rear panel of the logic analyzer.
3. Disconnect the logic analyzer cables from the rear panel. Remove the logic analyzer cables (and spacers, if installed) from the logic analyzer.
4. Using a Torx T-15 screwdriver, remove the screws connecting the four rear feet to the instrument, one screw per foot. Remove each foot from the rear panel.
5. Using a Torx T-10 screwdriver, remove eleven screws that secure the sleeve to the chassis.
6. With the logic analyzer upright, slide the chassis out of the sleeve.

7 Reverse this procedure to install the chassis into the sleeve.

When reassembling, check the following:

all assemblies are properly installed before installing the chassis into the sleeve.

ensure all exposed cables are dressed properly so the sleeve does not cause any damage to the cables.



To remove the acquisition board

1 Do the procedure "To remove the chassis from the sleeve".

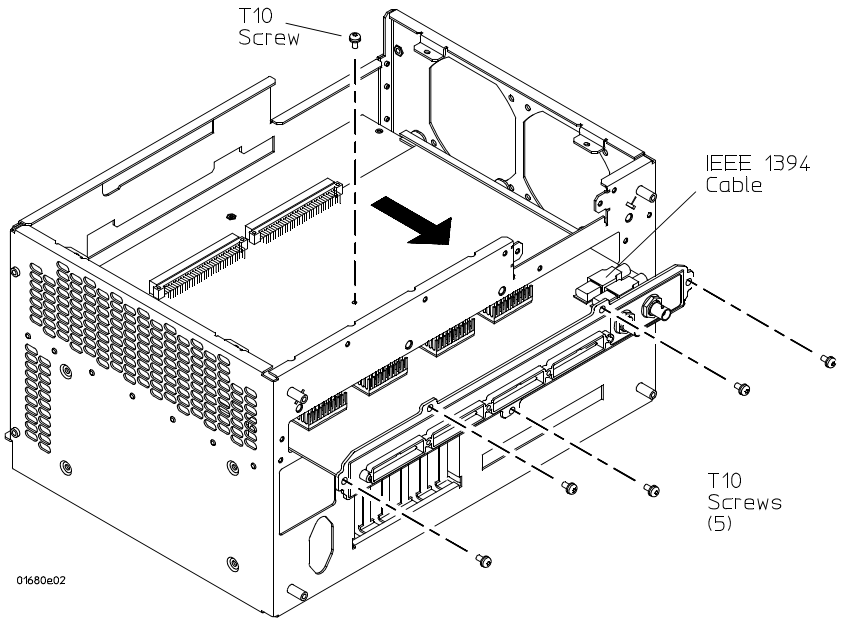
2 Turn the chassis upside down.

3 Disconnect the IEEE 1394 cable from the acquisition board.

4 Using a Torx T-10 screwdriver, remove five screws that secure the probe shroud to the rear panel of the logic analyzer.

5 Using a Torx T-10 screwdriver, remove one screw that secures the acquisition board to the chassis (center of the acquisition board).

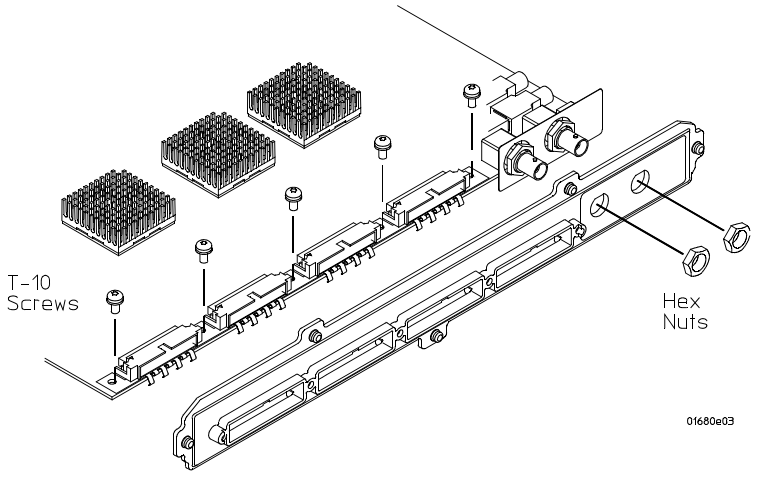
6 Slide the acquisition board out the rear panel of the logic analyzer.



Steps to remove probe shroud from acquisition board.

7 Using a hex screwdriver, remove two hex nuts from the acquisition board trigger BNC connectors.

8 Using a Torx T-10 screwdriver, remove five screws that secure the probe shroud to the acquisition board.

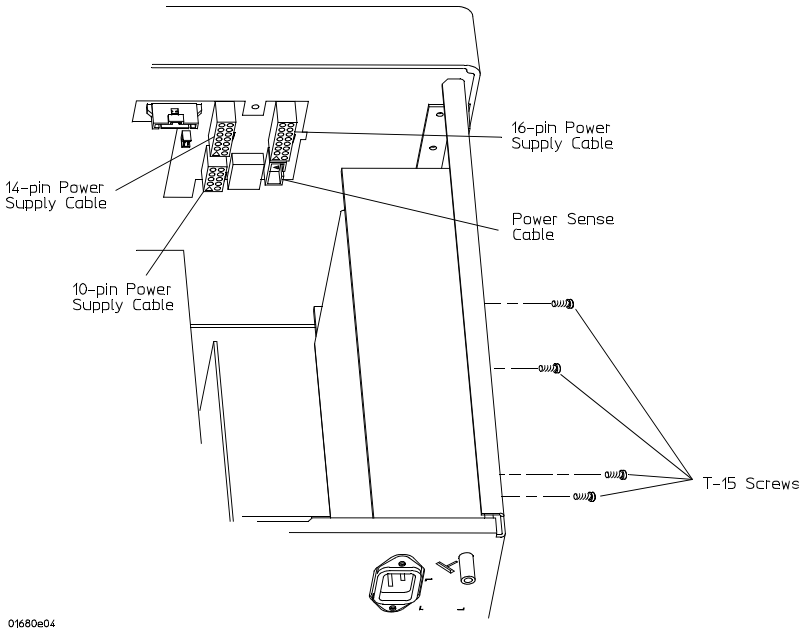


Reverse this procedure to install the acquisition board.

If the probe shroud requires replacing, then the probe shroud label (part number 01680-94312) must also be ordered and installed on the replacement probe shroud.

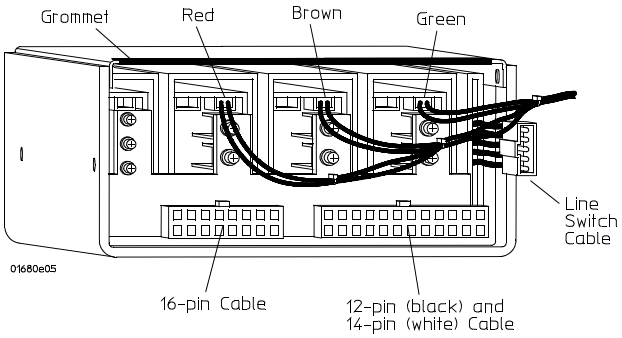
To remove the power supply

1. Do the procedure "To remove the chassis from the sleeve".
2. Disconnect the 16-pin power supply cable and the power sense cable from the distribution board.
3. Using a Torx T-15 screwdriver, remove four screws that secure the power supply to the chassis.
4. Lift the power supply out of the chassis.
5. Disconnect the 14-pin and the 10-pin power supply cables from the distribution board.



6 Reverse this procedure to install the power supply

When installing a replacement power supply, transfer the power supply cables and the grommet to the replacement power supply as shown:



To remove the hard disk drive

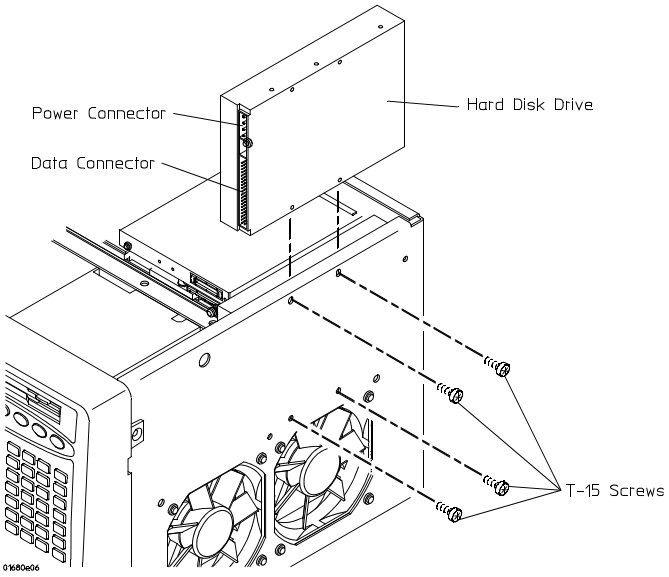
1 Do the procedure "To remove the chassis from the sleeve".

2 Using a Torx T-15 screwdriver, remove four screws that secure the hard disk drive to the chassis.

3 Lift the hard disk drive out of the chassis.

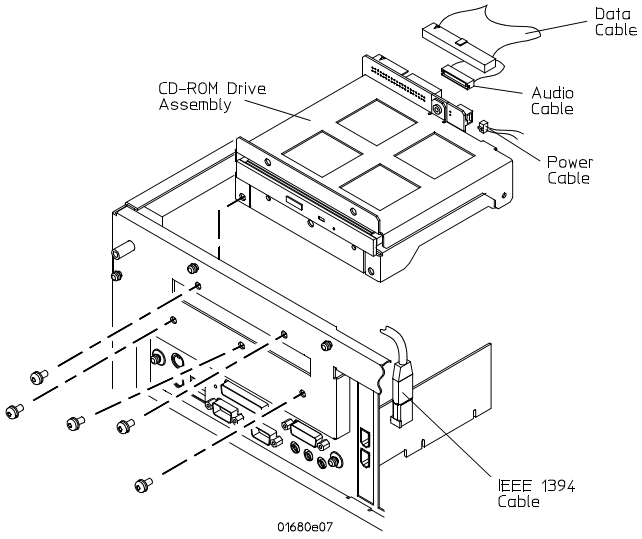
4 Disconnect both the power cable and the data cable from the hard disk drive.

5 Reverse this procedure to install the hard disk drive.



To remove the CD-ROM drive assembly

1. Do the procedure "To remove the chassis from the sleeve".
2. Disconnect the IEEE 1394 cable from the PCI IEEE 1394 interface board. Disengage the cable from the cable clamps on the top of the CD-ROM drive assembly.
3. Remove the data cable, power cable and audio cable from the CD-ROM drive interface board.
4. Using a Torx T-10 screwdriver, remove five screws that secure the CD-ROM drive assembly to the chassis.
5. Slide the CD-ROM assembly out of the chassis.

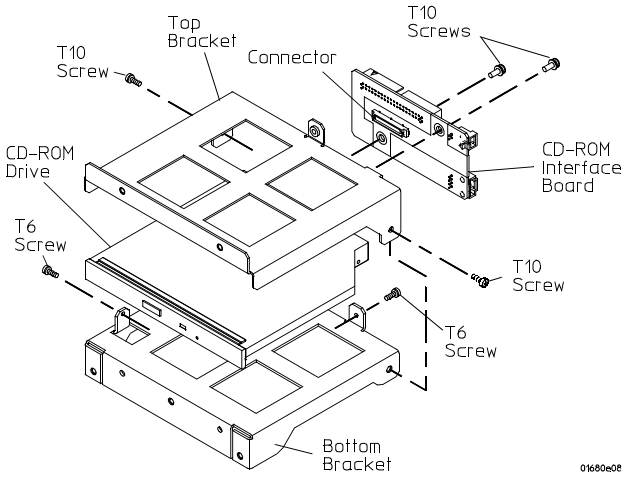


Remove the CD-ROM from the assembly

1. 1 Using a Torx T-10 screwdriver, remove two screws that secure the CD-ROM interface board to the CD-ROM drive brackets.
2. Remove the interface board from the CD-ROM drive brackets.

   A connector on the back of the CD-ROM interface board will disengage from an interface connector on the rear of the CD-ROM drive.
3. Using a Torx T-10 screwdriver, remove two screws, one on each side of the CD-ROM drive brackets, that secure the top bracket to the bottom bracket. Separate the two brackets.

4 Using a Torx T-6 screwdriver, remove three screws that secure the CD-ROM drive to the bottom bracket. Lift the CD-ROM drive out of the bottom bracket.

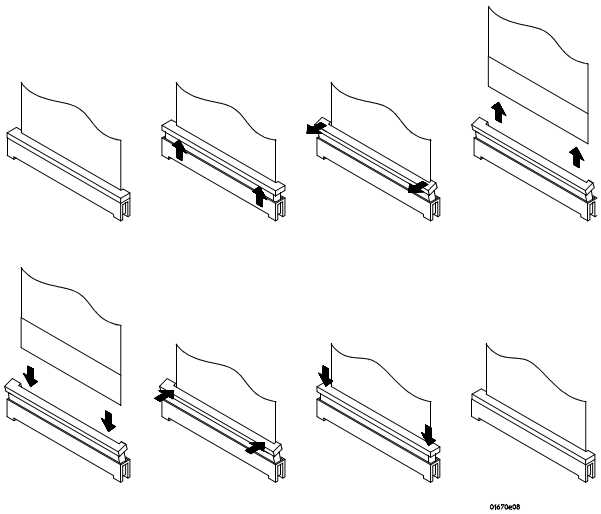


5 Reverse this procedure to reassemble and install the CD-ROM drive. Ensure the motherboard is properly installed before installing the CD-ROM drive.

To remove the flexible disk drive

1 Do the procedure "To remove the chassis from the sleeve".

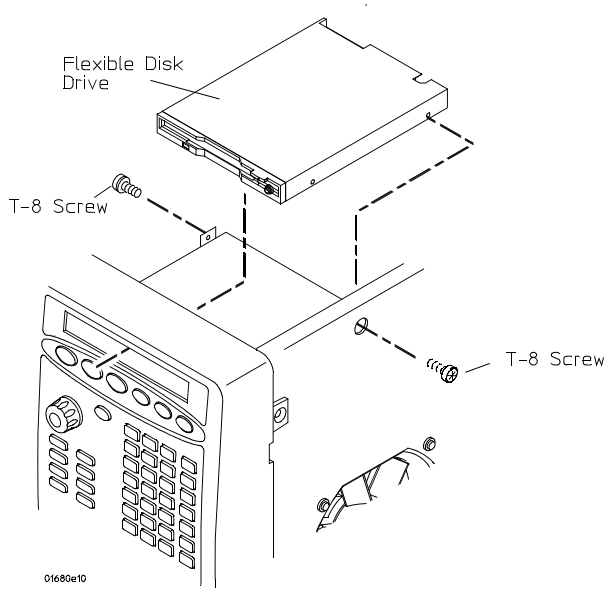
2 Unplug the flexible disk drive cable from the rear of the flexible disk drive.



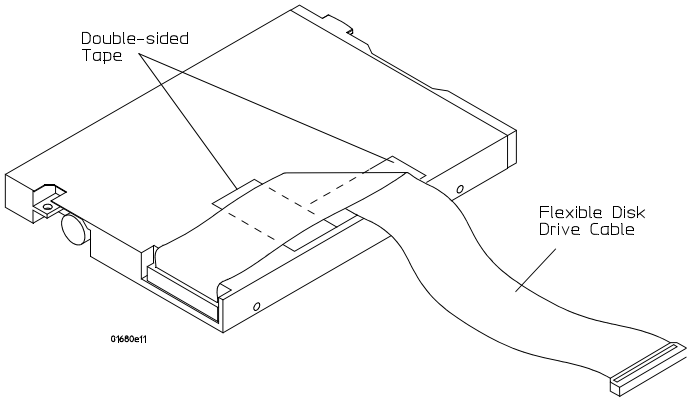
3 Using a Torx T-8 screwdriver, remove two screws that secure the flexible disk drive to the chassis.

4 Slide the flexible disk drive out the rear of the front panel and out of the chassis.

5 Reverse this procedure to install the flexible disk drive.



When installing a new flexible disk drive, industrial double-sided tape (Agilent 0460-2010 or similar) is required to dress the cable onto the flexible disk drive. Apply the tape as shown.



To remove the PCI boards

The following PCI boards are installed on the logic analyzer motherboard:

PCI IEEE 1394 board (slot 2, closest to the CD-ROM drive)

PCI display board (slot 3)

slot covers (slot 3 and slot 4)

1 Do the procedure "To remove the chassis from the sleeve".

2 Disconnect the cable from the board to be removed:

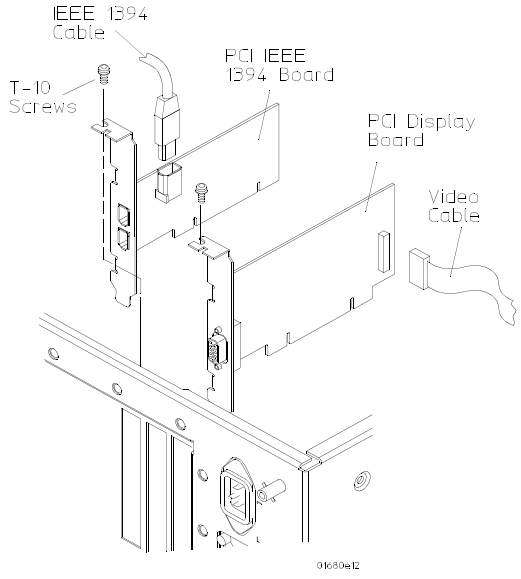
PCI IEEE 1394 board: IEEE 1394 cable

PCI display board: video cable

3 Using a Torx T-10 screwdriver, remove one screw that secures each PCI board to the rear panel.

4 Slide each board out the top of the chassis.

If the PCI display board is replaced, check to see if tape is covering the video cable connector on the board. If tape covers the connector, remove the tape before installing the PCI display board onto the motherboard.



5 Reverse this procedure to install the PCI boards.

To remove the motherboard

1. Do the procedure "To remove the chassis from the sleeve".
2. Do the procedure "To remove the CD-ROM drive" .
3. Remove both PCI peripheral boards from the motherboard using the procedure "To remove the PCI boards."
4. Disconnect the following cables from the motherboard:

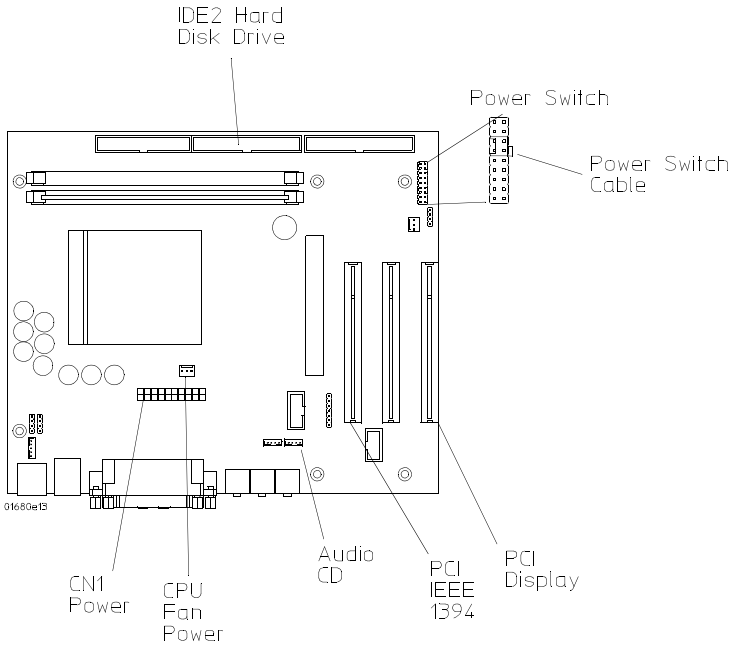
   power switch cable from motherboard J1 pins 6 and 8

   hard disk drive cable from connector FDD1

   power cable from connector CN1

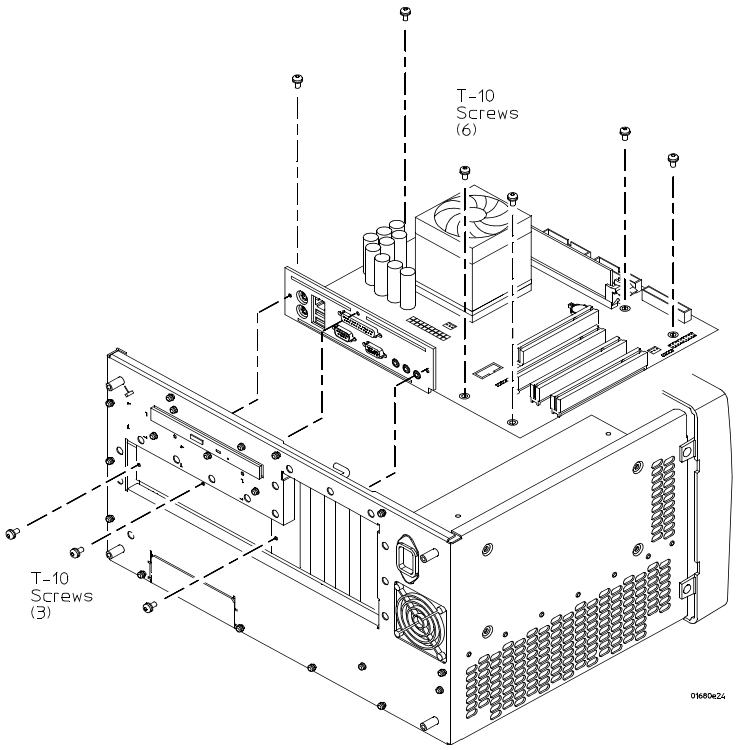
   CPU fan cable

   audio cable from connector CD



5. Using a Torx T-10 screwdriver, remove the 3 screws that secure the motherboard back plate to the rear panel.

6 Using a Torx T-10 screwdriver, remove the 6 screws that secure the motherboard to the chassis.



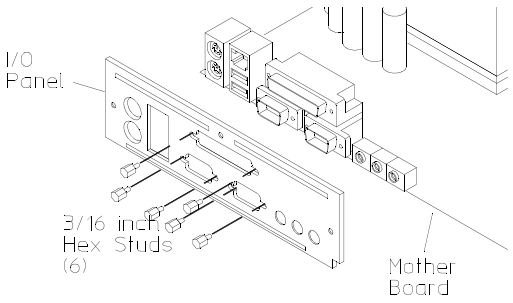
7 Reverse this procedure to install the motherboard.

If the motherboard requires replacing, then do the following steps:

Transfer the I/O panel to the replacement board

1 Using a 3/16 inch hex nut driver, remove 6 hex studs that secure the I/O panel to the parallel port, VGA port and COM1 port.

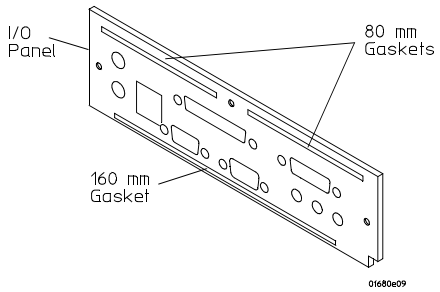
2 Remove the I/O panel from the motherboard.



3 If the I/O panel requires replacement, then EMI gasket (01680-87102) must be installed into the replacement I/O panel. The gasket is installed as follows:

a Two 80 mm sections are installed, one on each side of the top center screw hole.

b One 160 mm section is installed centered along the bottom edge of the I/O panel directly beneath the keyboard, USB, COM1, VGA and audio ports.



4 Install the I/O panel onto the replacement motherboard. (Shown in step 2 on previous page.)

5 Install 6 hex studs onto the motherboard ports and tighten.

To remove the front panel assembly

1 Do the procedure "To remove the chassis from the sleeve".

2 Using diagonal cutters, cut the tie wrap off the on/off cable.

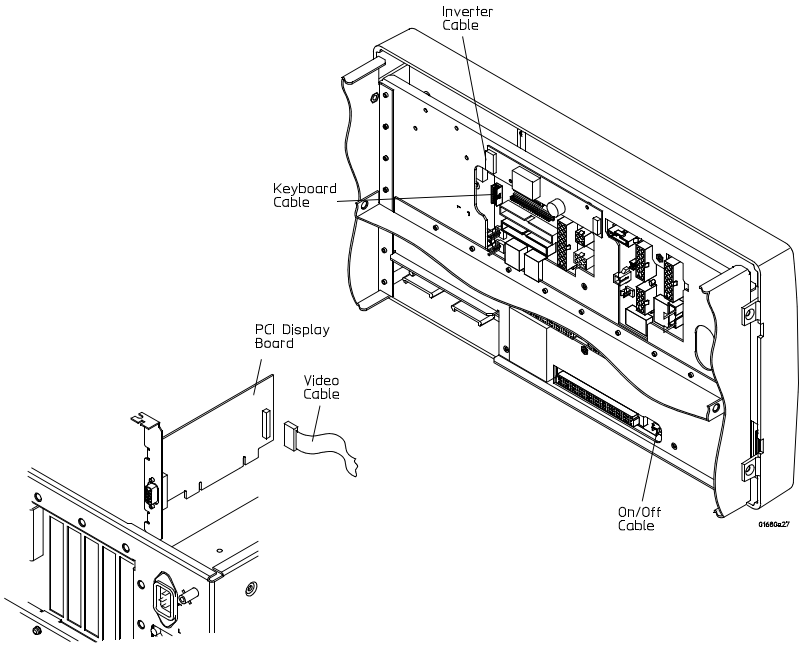
3 Disconnect the display cable from the PCI display board.

4 Disconnect the following cables from the distribution board:

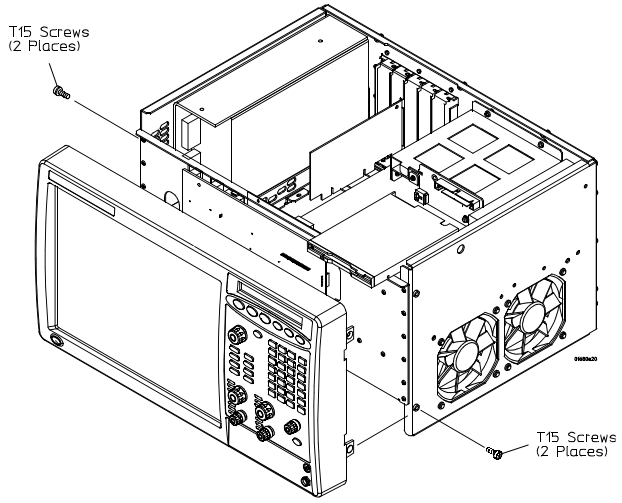
on/off cable (accessed from the bottom of the chassis)

keyboard cable

inverter cable

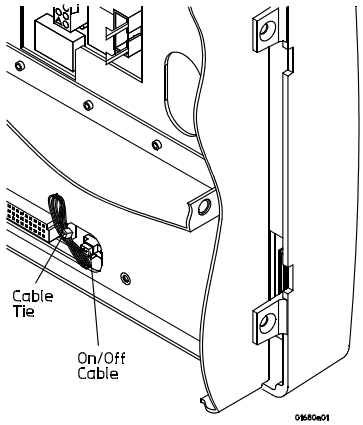


5 Using a Torx T-15 screwdriver, remove four screws that secure the front panel assembly to the chassis. Lift the front panel assembly away from the chassis.

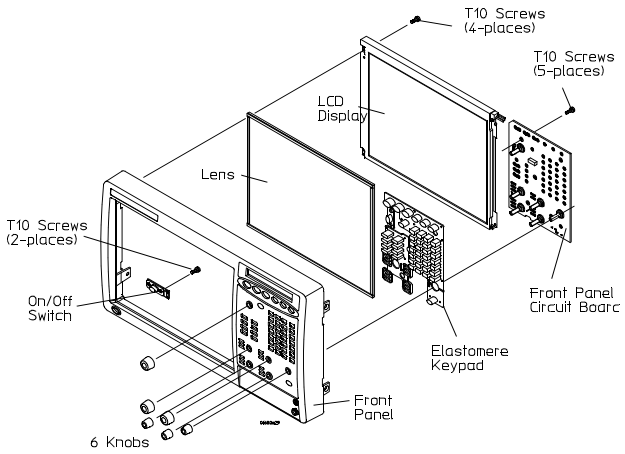


6 Reverse this procedure to install the front panel assembly.

After installing the front panel assembly onto the chassis, loop the on/off cable and dress the cable with a cable tie (Agilent part number 1400-0249 or similar). Dressing the cable with a cable tie ensures the cable will not be caught in the sleeve when the chassis is slid into the sleeve during assembly.



To disassemble the front panel assembly



Remove the front panel circuit board.

1 Remove each of the knobs from the front panel.

2 Using a Torx T-10 screwdriver, remove five screws that secure the front panel circuit board to the front panel.

3 Lift the front panel circuit board out of the front panel.

4 Lift the elastomeric keypad out of the front panel.

Remove the LCD display.

1 Using a Torx T-10 screwdriver, remove four screws, one in each corner, that secures the LCD display to the front panel.

2 Lift the LCD display out of the front panel.

3 Lift the glass lens out of the front panel assembly.

NOTE: When installing, blow any dust off of the LCD and lens.

Remove the on/off switch.

1 Using a Torx T-10 screwdriver, remove two screws that secure the on-off switch circuit board to the front panel.

2 Lift the on/off switch circuit board out of the front panel.

3 Lift the on/off switch out of the front panel.

Reverse this procedure to assemble the front panel assembly.

If the front panel requires replacement, a product ID label must also be ordered and applied (refer to chapter 7 for the part number).

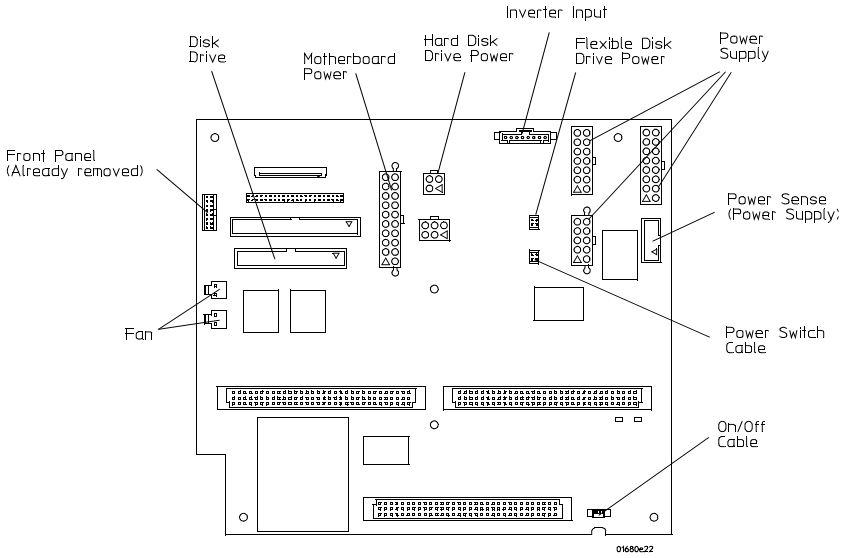
To remove the distribution board

1 1 Do the following procedures:

To remove the chassis from the sleeve

To remove the front panel assembly

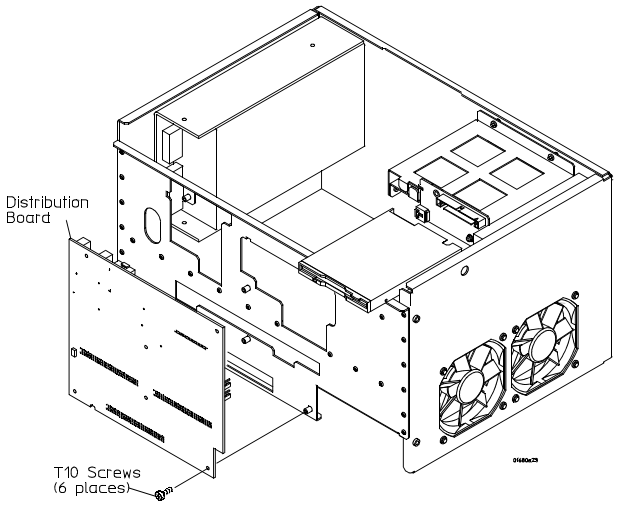
2 Disconnect all cables from the distribution board as shown.



3 Using a Torx T-10 screwdriver, remove six screws that secure the distribution board to the chassis.

4 Lift the distribution board away from the chassis.

5 Reverse this procedure to install the distribution board.



To remove the inverter board

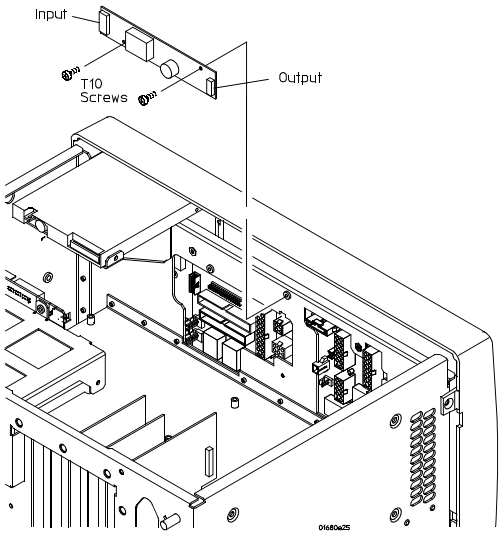
1 Do the procedure "To remove the chassis from the sleeve".

2 Disconnect both the inverter input and inverter LCD inverter output cables from the inverter board.

3 Using a Torx T-10 screwdriver, remove two screws that secure the inverter board to the chassis.

4 Lift the inverter board out of the chassis.

5 Reverse this procedure to install the inverter board.



To remove the fans

1 Do the procedure "To remove the chassis from the sleeve".

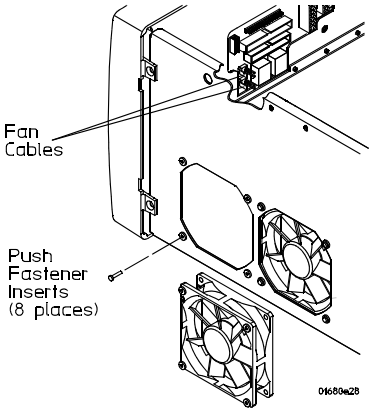
2 Disconnect the fan cables from the distribution board.

3 Using needle-nosed pliers, remove the plastic push fastener insert from the push fasteners securing one of the fans to the chassis.

4 Disengage the fan from the push fasteners and remove the fan through the bottom of the chassis.

5 If necessary, repeat steps 2 through 4 for the remaining fan.

6 Reverse this procedure to install the fans.



To remove the cable tray

Do the following steps only if the cable tray requires replacement.

If the cable tray requires replacing, then a label must also be ordered and applied to the cable tray depending on the 1680A,AD-series instrument the cable tray is installed on:

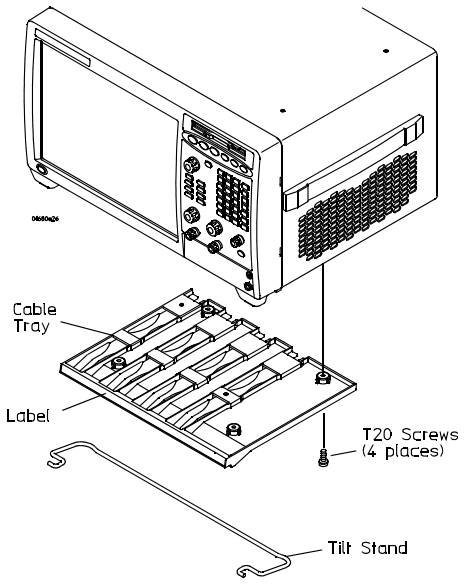
1680A,AD: 01680-94307

1681A,AD: 01680-94308

1682A,AD: 01680-94309

1683A,AD: 01680-94310

1. Remove the tilt stand from the bottom front feet.
2. Remove the logic analyzer cables from the cable tray
3. Using a Torx T-20 screwdriver, remove four screws that secure the cable tray to the sleeve.
4. Reverse this procedure to install the cable tray.



1690A,AD-series disassembly/assembly

Prepare the instrument for disassembly

Do this procedure before doing any disassembly procedure on the instrument.

1. Close the Agilent Logic Analyzer application software.
2. Disconnect the logic analyzer from the host PC.
3. Remove power and disconnect the power cord.
4. Move the instrument to a static safe work environment.

To remove the chassis from the sleeve

Before disassembling the instrument, it must be turned off and placed in a static safe work environment. If you haven't already done so, do the previous procedure "Prepare the instrument for disassembly."

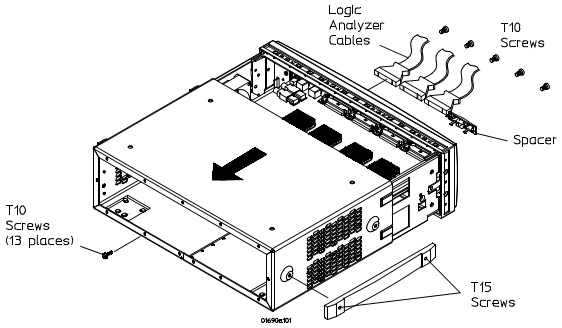
1. Using a Torx T-15 screwdriver, remove the two screws that secure the handle to the side of the instrument and lift off the handle.
2. Using a Torx T-10 screwdriver, remove five screws that secure the logic analyzer cables (and spacers, if installed) to the front panel of the logic analyzer.
3. Disconnect the logic analyzer cables from the front panel. Remove the logic analyzer cables (and spacers, if installed) from the logic analyzer.
4. Using a Torx T-10 screwdriver, remove thirteen screws that secure the cover to the chassis.
5. With the logic analyzer upright, slide the chassis out of the cover.

6 Reverse this procedure to install the chassis into the sleeve.

When reassembling, check the following:

all assemblies are properly installed before installing the chassis into the sleeve.

ensure all exposed cables are dressed properly so the sleeve does not cause any damage to the cables.

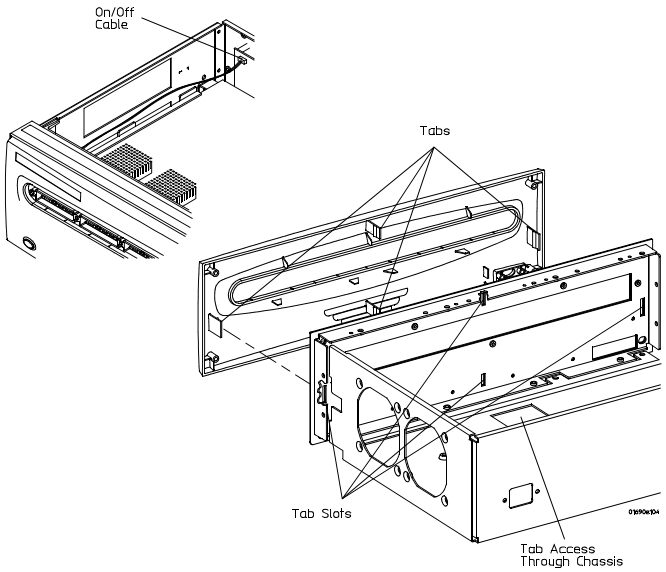


To remove the fascia

1 Do the procedure "To remove the chassis from the sleeve".

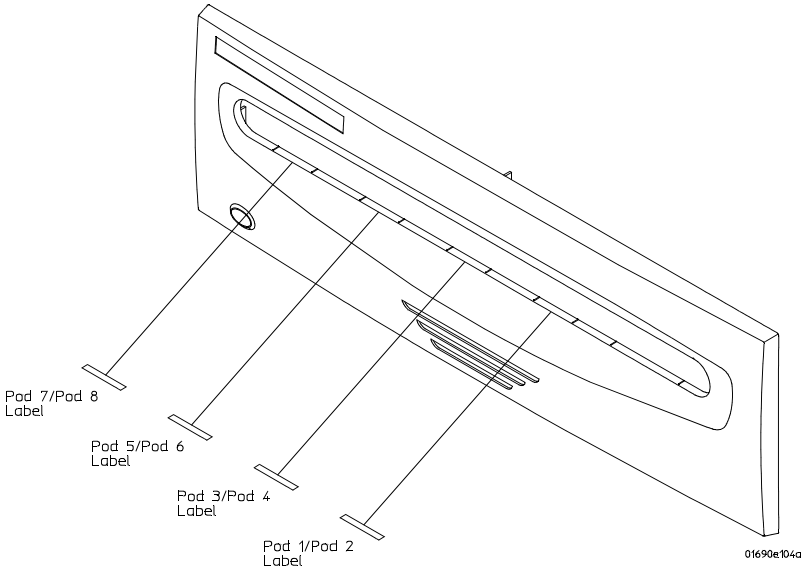
2 Disconnect the on/off cable from the distribution board and remove the cable from the cable clip.

3 Disengage the four tabs in the inside of the front panel that secure the fascia to the front panel.



4 Remove the fascia away from the front panel.

If the fascia requires replacement, a product ID label must also be ordered and applied (refer to chapter 7 for the part number). Also, Pod labels (01680-94313) must be ordered and applied in the same way as on the fascia being replaced.

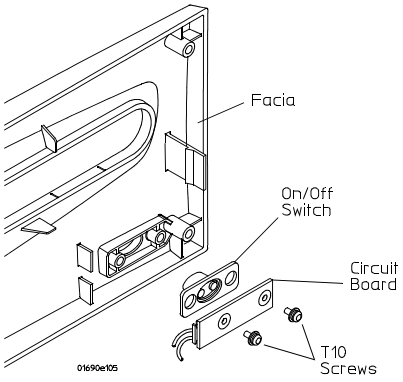


Steps to remove the on/off switch from the fascia assembly

1 Using a Torx T-10 screwdriver, remove two screws that secure the on-off switch circuit board to the fascia.

2 Lift the on/off switch circuit board out of the fascia.

3 Lift the on/off switch out of the fascia.



Reverse this procedure to assemble the fascia.

To remove the acquisition board

1 Do the following procedures:

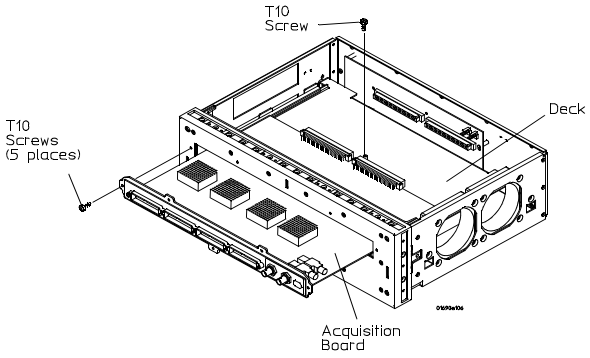
To remove the chassis from the sleeve

To remove the fascia

2 Using a Torx T-10 screwdriver, remove one screw that secures the acquisition board to the deck.

3 Using a Torx T-10 screwdriver, remove five screws that secure the probe shroud to the logic analyzer front panel.

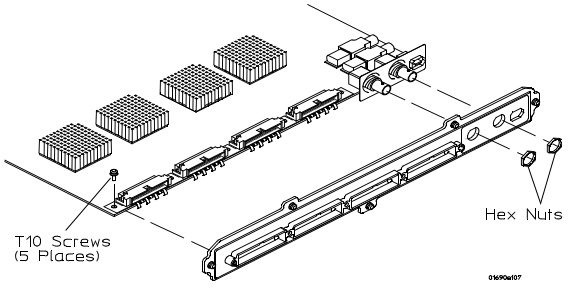
4 Slide the acquisition board out of the logic analyzer front panel.



Steps to remove the probe shroud from the acquisition board.

1 Using a hex screwdriver, remove two hex nuts from the acquisition board trigger BNC connectors.

2 Using a Torx T-10 screwdriver, remove five screws that secure the probe shroud to the acquisition board.



Reverse this procedure to install the acquisition board

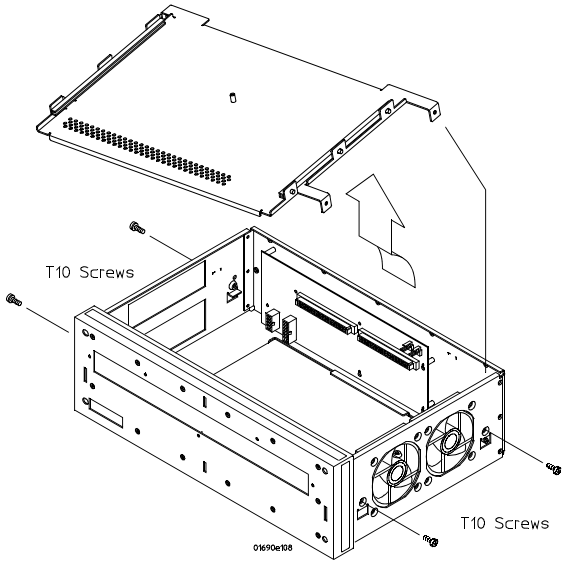
If the probe shroud requires replacing, then the probe shroud label (part number 01690-94302) must also be ordered and installed on the replacement probe shroud.

To remove the deck

1 Using a Torx T-10 screwdriver, remove four screws that secure the deck to the chassis.

2 Tilt the rear of the deck up and out of the chassis.

3 Lift the deck up and away from the chassis.



To remove the power supply

1 Do the following procedures:

To remove the chassis from the sleeve

To remove the front panel assembly

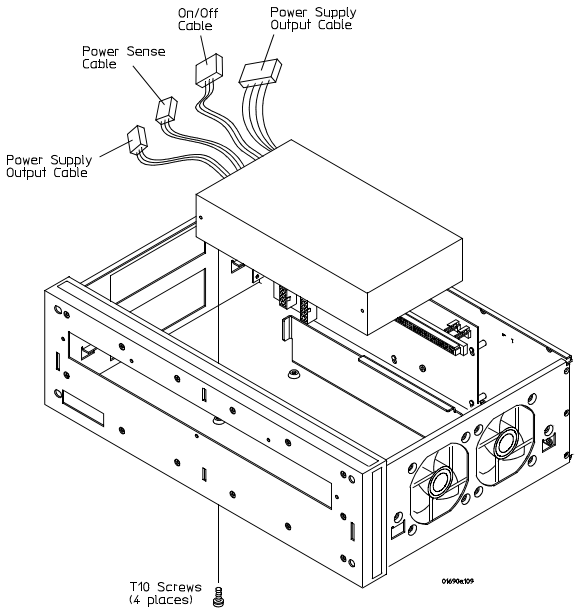
To remove the deck

2 Disconnect the power supply output cables, the on/off cable and the power sense cable from the distribution board.

3 Disconnect the power supply line input cable from the power supply.

4 Using a Torx T-10 screwdriver, remove four screws that secure the power supply to the bottom of the chassis.

5 Lift the power supply out of the chassis.



6 Reverse this procedure to install the power supply

When installing a replacement power supply, transfer both the power sense cable and the power supply on/off cable to the replacement power supply.

To remove the distribution board

1 Do the following procedures:

To remove the chassis from the sleeve

To remove the front panel assembly

To remove the deck

2 Disconnect the following cables from the distribution board:

power supply output cables (P1, P2)

on/off cable (P3)

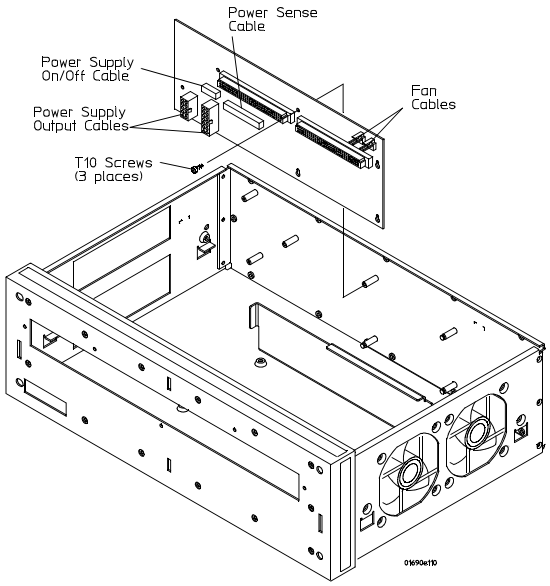
power sense cable (P7)

fan cables (P5, P6)

3 Using a Torx T-10 screwdriver, remove three screws that secure the distribution board to the chassis.

4 Slide the distribution board up approx 1 cm, then lift the board away from the chassis.

5 Reverse this procedure to install the distribution board.



To remove the fans

1 Do the procedure "To remove the chassis from the sleeve".

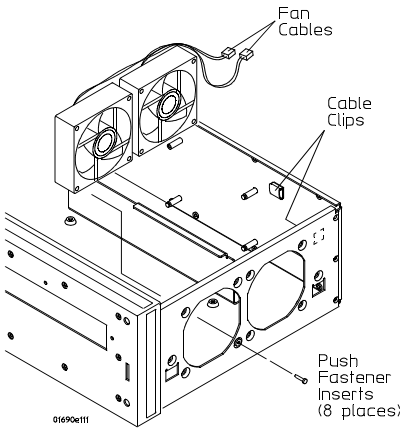
2 Disconnect the fan cables from the distribution board and remove the cables from the cable clips.

3 Using needle-nosed pliers, remove the plastic push fastener insert from the push fasteners securing one of the fans to the chassis.

4 Disengage the fan from the push fasteners and remove the fan out the top of the chassis.

5 If necessary, repeat steps 2 through 4 for the remaining fan.

6 Reverse this procedure to install the fans.



To remove the line filter

1 Do the following procedures:

To remove the chassis from the sleeve

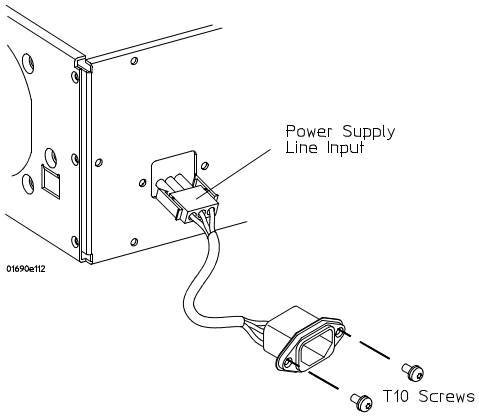
To remove the front panel assembly

To remove the deck

2 Disconnect the power supply line input cable from the power supply.

3 Using a Torx T-10 screwdriver, remove two screws that secure the line filter to the rear of the chassis.

4 Remove the line filter out the rear of the chassis.



To remove the front panel and front frame

1 Do the following procedures:

To remove the chassis fron the sleeve

To remove the fascia

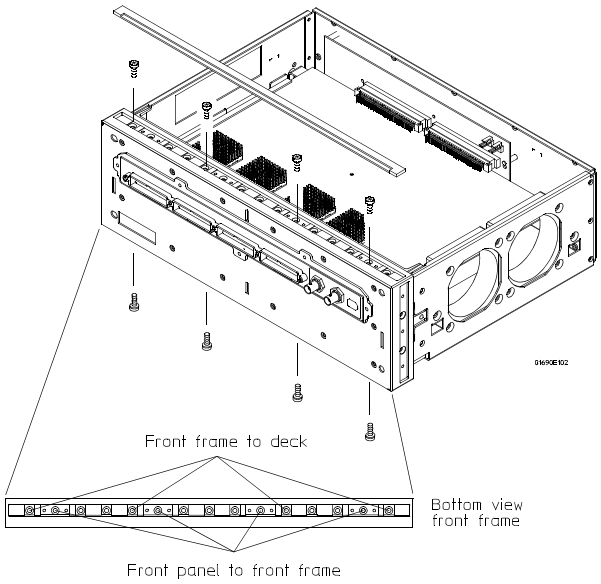
To remove the acquisition board

2 Remove the trim strips from the top and sides of the front frame.

3 Using a Torx T-15 screwdriver remove four screws that secure the top of the front panel to the front frame.

4 Using a Torx T-15 screwdriver, remove four screws that secure the bottom of the front panel to the front frame, as shown.

5 Using a Torx T-15 screwdriver, remove four screws that secure the front frame to the deck.



7

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analyzer.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and there are no invoices.

For Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also "To return assemblies," in chapter 6.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

The exploded view does not show all of the parts in the replaceable parts list.

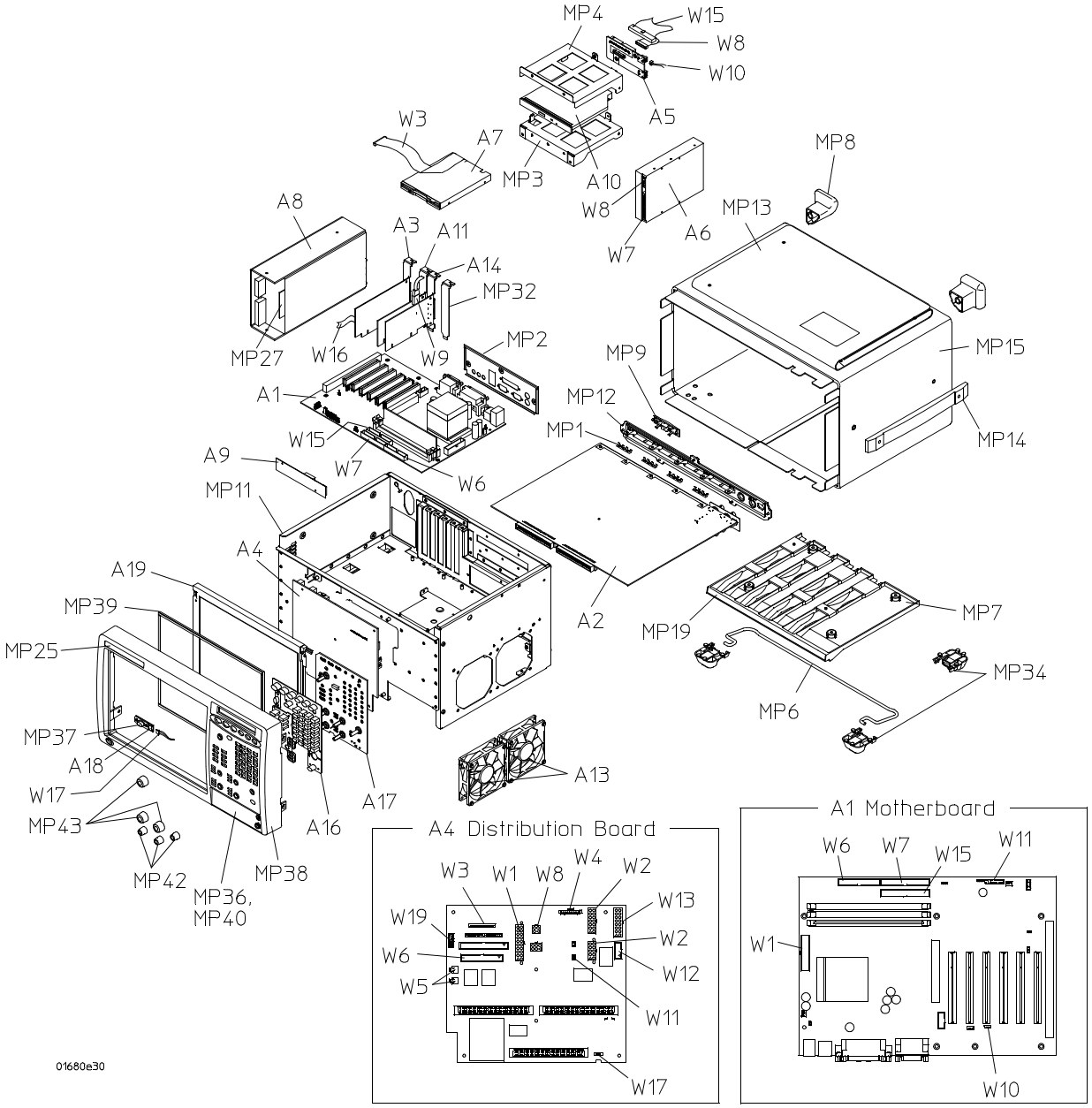
Information included for each part on the list consists of the following:

- Reference designator
- Agilent Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- E Miscellaneous Electrical Part
- F Fuse
- H Hardware
- MP Mechanical Part
- W Cable

Exploded View



Exploded view of the Agilent 1680A,AD-series logic analyzer

Agilent 1680A,AD-Series Replaceable Parts

Replaceable Parts			
Ref. Des.	**Agilent Part Number**	**QTY**	**Description**
Exchange Assemblies			
	01680-69603		Motherboard Assembly
	16600-69600		Power Supply
	01680-69507		Acquisition Board 136 Channel x 2 Mbit (1680AD)
	01680-69508		Acquisition Board 34 Channel x 2 Mbit (1693AD)
	01680-69509		Acquisition Board 68 Channel x 2 Mbit (1692AD)
	01680-69510		Acquisition Board 102 Channel x 2 Mbit (1691AD)
	01680-69517		Acquisition Board 34 Channel x 512 Kbit (1693A)
	01680-69518		Acquisition Board 68 Channel x 512 Kbit (1692A)
	01680-69519		Acquisition Board 102 Channel x 512 Kbit (1691A)
	01680-69520		Acquisition Board 136 Channel x 512 Kbit (1690A)
Replacement Parts			
A2	01680-66507	1	Acquisition Board 136 Channel x 2 Mbit (1680AD)
A2	01680-66508	1	Acquisition Board 34 Channel x 2 Mbit (1693AD)
A2	01680-66509	1	Acquisition Board 68 Channel x 2 Mbit (1692AD)
A2	01680-66510	1	Acquisition Board 102 Channel x 2 Mbit (1691AD)
A2	01680-66517	1	Acquisition Board 34 Channel x 512 Kbit (1693A)
A2	01680-66518	1	Acquisition Board 68 Channel x 512 Kbit (1692A)
A2	01680-66519	1	Acquisition Board 102 Channel x 512 Kbit (1691A)
A2	01680-66520	1	Acquisition Board 136 Channel x 512 Kbit (1690A)
A3	01680-66501	1	PCI Display Board
A4	01680-66504	1	Power Distribution Board
A5	01680-66530	1	CD-ROM Interface Board
A6	01680-83513	1	Hard Disk Drive with Software
A7	0950-2782	1	Flexible Disk Drive
A8	0950-3403	1	Power Supply
A9	0950-4068	1	Inverter
A10	0950-4373	1	CD-ROM Drive
A12	1150-7809	1	Mini Keyboard
A13	3160-0818	2	Fan
A14	0960-2453	1	PCI IEEE 1394 Board
A15	1150-7845	1	Mouse
E2	16542-61607	1	Double Probe Adapter
E3	5090-4833	8	Grabber Kit Assembly (1680A, AD)

Replaceable Parts			
Ref. Des.	**Agilent Part Number**	**QTY**	**Description**
E3	5090-4833	6	Grabber Kit Assembly (1681A, AD)
E3	5090-4833	4	Grabber Kit Assembly (1682A, AD)
E3	5090-4833	2	Grabber Kit Assembly (1683A, AD)
E4	5959-9333	0	Replacement Probe Leads (Qty 5)
E5	5959-9335	0	Replacement Pod Grounds - 5" (Qty 2)
E6	5959-9334	8	Probe Grounds - 2" (Qty 5, 1680A, AD)
E6	5959-9334	6	Probe Grounds - 2" (Qty 5, 1681A, AD)
E6	5959-9334	4	Probe Grounds - 2" (Qty 5, 1682A, AD)
E6	5959-9334	2	Probe Grounds - 2" (Qty 5, 1683A, AD)
H1	0380-1927	6	Hex Standoff 0.185 in (I/O panel to motherboard ports)
H2	0515-0365	3	M2.0 x 0.40; 4 mm T6 PH (CD-ROM drive to CD-ROM drive bracket)
H3	0515-0372	40	M3.0 x 0.50; 8 mm T10 PH (I/O panel to chassis, module cover to chassis, CD-ROM top bracket to CD-ROM bottom bracket, distribution board to chassis, probe shroud to acquisition board, acquisition board to chassis, probe shroud to chassis, PCI board and ISA slot covers to chassis, CD-ROM drive assembly to chassis, sleeve to chassis)
H4	0515-0433	12	M4.0 x 0.70; 8 mm T20 PH (power supply to chassis, cable tray to sleeve, rear feet to chassis)
H5	0515-1403	8	M4.0 x 0.70; 6 mm T15 90° FH (snap to sleeve (accessory pouch), front panel assembly to chassis)
H6	0515-1934	2	M2.5 x 0.45; 6 mm T8 PH (inverter to chassis)
H7	0515-1974	2	M2.5 x 0.45; 4 mm T8 PH (flexible disk drive to chassis)
H8	0515-2306	5	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1680A, AD)
H8	0515-2306	4	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1681A, AD)
H8	0515-2306	3	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1682A, AD)
H8	0515-2306	2	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1680A, AD)
H9	2360-0452	4	6-32 0.250 in T15 PH with washer (hard disk drive to chassis)
H10	2950-0054	2	Hex Nut 0.625 x 0.125; 1/2-28 (acquisition board BNC connectors to probe shroud)

Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
H11	0515-0430	6	M3.0 x 5.0; 6 mm T10; motherboard to chassis
MP1	01660-09101	4	Ground Spring (1680A, AD)
MP1	01660-09101	3	Ground Spring (1681A, AD)
MP1	01660-09101	2	Ground Spring (1682A, AD)
MP1	01660-09101	1	Ground Spring (1681A, AD)
MP2	01680-00201	1	I/O Panel
MP3	01680-01203	1	CD-ROM Bracket - Bottom
MP4	01680-01204	1	CD-ROM Bracket - Top
MP5	01680-04101	1	Rear Cover
MP6	01680-04701	1	Tilt Stand
MP7	01680-40401	1	Cable Tray
MP8	01680-41001	4	Rear Foot
MP9	01680-44101	1	Pod Cover (1681A, AD)
MP9	01680-44101	2	Pod Cover (1682A, AD)
MP9	01680-44101	3	Pod Cover (1683A, AD)
MP10	01680-52201	1	Front Cover
MP11	01680-60101	1	Chassis
MP12	01680-68701	1	Probe Shroud
MP13	01680-68702	1	Accessory Pouch
MP14	01680-68707	1	Handle Assembly
MP15	01680-68708	1	Sleeve Assembly
MP16	01680-87102	1	EMI Gasket (I/O panel to chassis)
MP17	01680-87103		EMI Gasket (probe shroud to chassis)
MP18	01680-88601		Adhesive stripe (EMI Gasket to probe shroud)
MP19	01680-94307	1	Cable Tray Label (1680A, AD)
MP19	01680-94308	1	Cable Tray Label (1681A, AD)
MP19	01680-94309	1	Cable Tray Label (1682A, AD)
MP19	01680-94310	1	Cable Tray Label (1683A, AD)
MP20	01680-94311	1	Label - Cable Installation
MP21	01680-94312	1	Label - Probe Shroud
MP22	01680-94313	1	Label - Pod and Cable
MP23	01680-94314	1	Label - Certification
MP24	01680-94315	1	Label - Rating
MP25	01680-94303	1	ID Label (1680A)
MP25	01680-94316	1	ID Label (1680AD)
MP25	01681-94301	1	ID Label (1681A)

Replaceable Parts

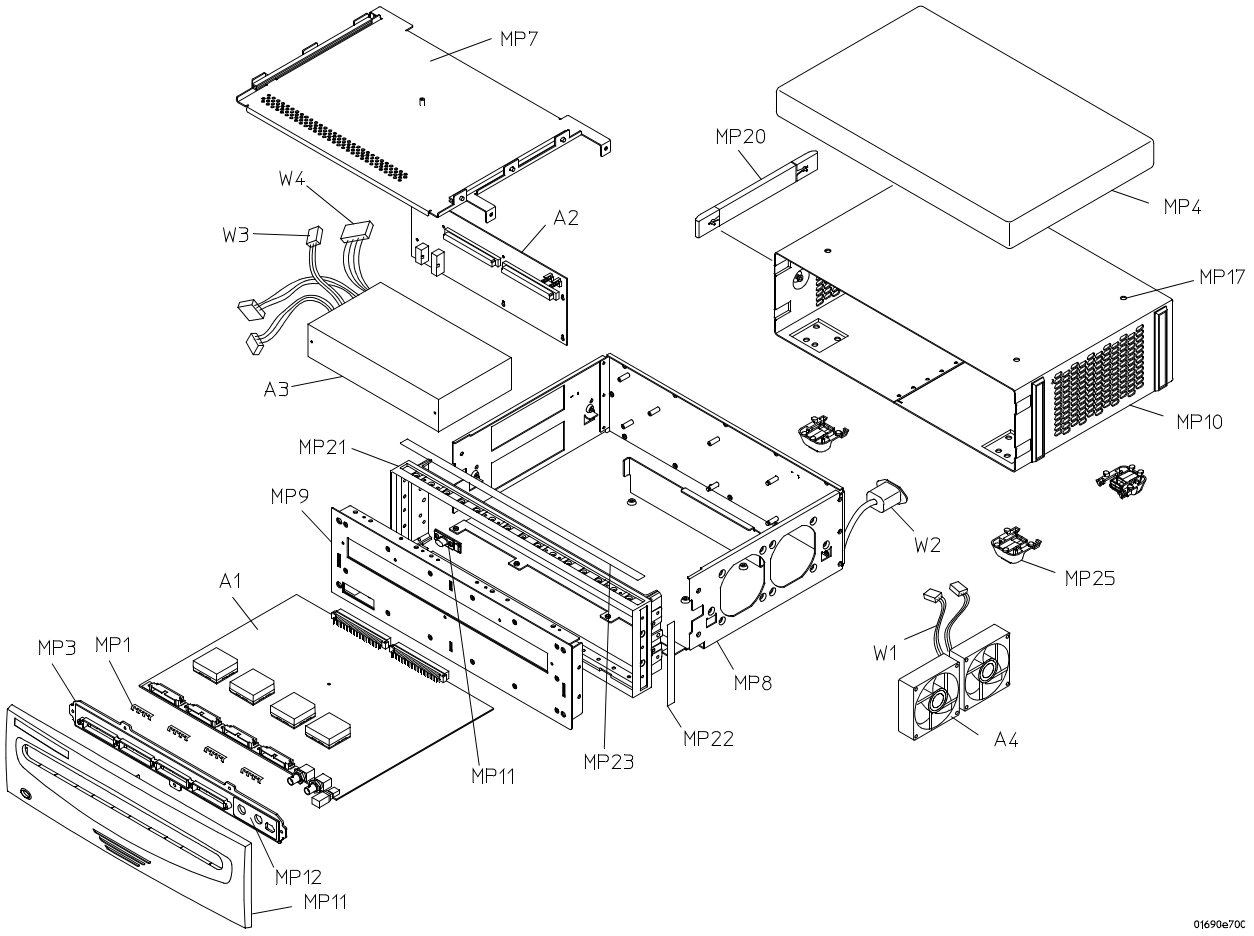
Ref. Des.	Agilent Part Number	QTY	Description
MP25	01681-94302	1	ID Label (1681AD)
MP25	01682-94301	1	ID Label (1682A)
MP25	01682-94302	1	ID Label (1682AD)
MP25	01683-94301	1	ID Label (1683A)
MP25	01683-94302	1	ID Label (1683AD)
MP26	0361-1787	8	Push Rivet (Fan to chassis)
MP27	0400-0727	0.35	Grommett, Stainless, Nylon Coated (front edge of power supply, chassis)
MP28	0400-0929	4	Snap (accessory pouch to sleeve)
MP29	0460-2010		Double-sided tape (flexible disk drive cable to flexible disk drive)
MP30	1400-0249		Cable Tie (motherboard cables, on/off cable)
MP31	1400-1254	2	Cable Clip 0.5 in diameter 0.75 in wide PVC (fan cables to chassis)
MP32	1400-2120	2	ISA Slot Cover
MP33	1400-3153	3	Cable Clamp (IEEE 1394 cable to CD-ROM assembly, IEEE 1394 cable to chassis)
MP34	54810-61001	4	Bottom Foot
MP35	8160-1545	0.65	EMI Gasket (I/O panel to chassis, CD-ROM assembly to chassis)
W1	01680-61604	1	PC Power Cable (distribution board to motherboard)
W2	01680-61605	1	Power Supply Cable (14- and 10- pin power supply output)
W3	01680-61606	1	Flexible Disk Drive Cable (distribution board to flexible disk drive)
W4	01680-61608	1	Inverter Cable (distribution board to inverter board)
W5	01680-61609	2	Fan Cable
W6	01680-61612	1	Flexible Disk Drive Cable (distribution board to motherboard)
W7	01680-61613	1	Disk Drive Data Cable (hard disk drive to motherboard)
W8	01680-61614	1	Hard Disk Drive Power Cable
W9	01680-61619	1	IEEE 1394 6-pin Cable (acquisition board to PCI IEEE 1394 board)
W10	01680-61622	1	Audio Cable (CD-ROM drive to motherboard)
W11	01680-61623	1	PC Sequence Cable (on/off, motherboard to distribution board)

Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
W12	16600-61602	1	Power Sense Cable (power supply to distribution board)
W13	16700-61604	1	Power Supply Cable (16-pin power supply output)
W14	16715-61601	4	Probe Cable (1680A, AD)
W14	16715-61601	3	Probe Cable (1681A, AD)
W14	16715-61601	2	Probe Cable (1682A, AD)
W14	16715-61601	1	Probe Cable (1683A, AD)
W15	54801-61611	1	Disk Drive Data Cable (CD-ROM drive to motherboard)
Front Panel Assembly			
A16	01680-41901	1	Keypad*
A17	01680-66502	1	Front Panel Circuit Board
A18	01680-66506	1	Power Switch Interface Board
A19	2090-0827	1	LCD Display
H11	0515-0372	9	M.30 x 0.50; 8 mm T10 PH (front panel circuit board to front frame, LCD display to front frame)
H12	0515-1934	2	M2.5 x 0.45; 6 mm T8 PH (power switch interface board to front frame)
MP36	01680-01702	1	Module Cover
MP37	01680-41901	1	On/Off Keypad*
* The front panel Keypad and On/Off Keypad are ordered together as one unit. When the Keypads are received, detach and use what is needed.			
MP38	01680-68712	1	Front Frame Assembly (includes the following
	01680-40501		Front Frame
	01680-94301		Front Panel Label
	54542-46101		Ground Lug
	0360-1646		Terminal Jack
	2190-0027		WIL.256 .478 .02 (ground lug to front frame)
	2950-0072		NUTH 1/4-32 .062 (ground lug to front frame)
MP39	01680-68713	1	Lens Assembly (includes the following)
	01680-87101		Lens Gasket
	01680-88001		Lens
MP40	01680-94302	1	Module Cover Label

Replaceable Parts			
Ref. Des.	**Agilent Part Number**	**QTY**	**Description**
MP41	1400-0611	1	Cable Clamp, 1 in x 1 in adhesive backed (LCD to LCD display)
MP42	54801-47401	3	Knob 12 MM Flint Gray
MP43	54801-47402	3	Knob 18 MM Gray
W16	01680-61602	1	Display Cable
W17	01680-61603	1	On/Off Cable
W18	01680-61611	1	Calibration Cable
W19	01680-61615	1	Front Panel Cable

Exploded View



Exploded view of the Agilent 1690A,AD-series logic analyzer

Agilent 1690A,AD-Series Replaceable Parts

Replaceable Parts			
Ref. Des.	**Agilent Part Number**	**QTY**	**Description**
Exchange Assemblies			
	01680-69507	1	Acquisition Board 136 Channel x 2 Mbit (1690AD)
	01680-69508	1	Acquisition Board 34 Channel x 2 Mbit (1693AD)
	01680-69509	1	Acquisition Board 68 Channel x 2 Mbit (1692AD)
	01680-69510	1	Acquisition Board 102 Channel x 2 Mbit (1691AD)
	01680-69517	1	Acquisition Board 34 Channel x 512 Kbit (1693A)
	01680-69518	1	Acquisition Board 68 Channel x 512 Kbit (1692A)
	01680-69519	1	Acquisition Board 102 Channel x 512 Kbit (1691A)
	01680-69520	1	Acquisition Board 136 Channel x 512 Kbit (1690A)
Replacement Parts			
A1	01680-66507	1	Acquisition Board 136 Channel x 2 Mbit (1690AD)
A1	01680-66508	1	Acquisition Board 34 Channel x 2 Mbit (1693AD)
A1	01680-66509	1	Acquisition Board 68 Channel x 2 Mbit (1692AD)
A1	01680-69510	1	Acquisition Board 102 Channel x 2 Mbit (1691AD)
A1	01680-69517	1	Acquisition Board 34 Channel x 512 Kbit (1693A)
A1	01680-69518	1	Acquisition Board 68 Channel x 512 Kbit (1692A)
A1	01680-69519	1	Acquisition Board 102 Channel x 512 Kbit (1691A)
A1	01680-69520	1	Acquisition Board 136 Channel x 512 Kbit (1690A)
A2	01680-66515	1	Distribution Board
A3	0950-4117	1	Power Supply (includes power supply output cables)
A4	3160-1006	2	Fan
E2	16542-61607	1	Double Probe Adapter
E3	5090-4833	8	Grabber Kit Assembly
E3	5090-4833	6	Grabber Kit Assembly
E3	5090-4833	4	Grabber Kit Assembly
E3	5090-4833	2	Grabber Kit Assembly
E4	5959-9333	0	Replacement Probe Leads (Qty 5)
E5	5959-9335	0	Replacement Pod Grounds - 5" (Qty 2)
E6	5959-9334	8	Probe Grounds - 2" (Qty 5)
E6	5959-9334	6	Probe Grounds - 2" (Qty 5)
E6	5959-9334	4	Probe Grounds - 2" (Qty 5)
E6	5959-9334	2	Probe Grounds - 2" (Qty 5)

Replaceable Parts

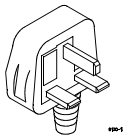
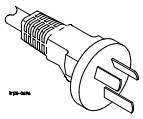
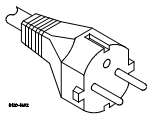
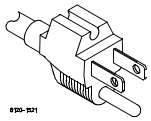
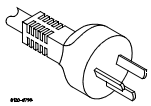
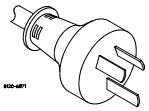
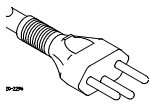
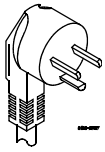
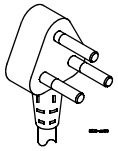
Ref. Des.	Agilent Part Number	QTY	Description
H1	0515-0372	31	M3.0 x 0.50; 8 mm T10 PH (distribution board to chassis, deck to chassis, probe shroud to acquisition board, acquisition board to deck, probe shroud to front panel, sleeve to chassis)
H2	0515-1035	2	M3.0 x 0.50; 8 mm T10 90° FH (line cable assembly to chassis rear)
H3	0515-1403	20	M4.0 x 0.70; 6 mm T15 90° FH (front panel to front frame, front frame to chassis, snap to sleeve (accessory pouch))
H4	0515-1934	2	M2.5 x 0.45; 6 mm T8 PH (power switch interface to fascia)
H5	0515-2306	5	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1690A, AD)
H6	0515-2306	4	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1691A, AD)
H6	0515-2306	3	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1692A, AD)
H6	0515-2306	2	M3.0 x 0.5; 10 mm T10 PH (probe cable to probe shroud, 1693A, AD)
H7	54503-25701	2	Hex Nut (acquisition board BNC connectors to probe shroud)
MP1	01660-09101	4	Ground Spring (1690A, AD)
MP1	01660-09101	3	Ground Spring (1691A, AD)
MP1	01660-09101	2	Ground Spring (1692A, AD)
MP1	01660-09101	1	Ground Spring (1693A, AD)
MP2	01680-44101	1	Pod Cover (1691A, AD)
MP2	01680-44101	2	Pod Cover (1692A, AD)
MP2	01680-44101	3	Pod Cover (1693A, AD)
MP3	01680-68701	1	Probe Shroud
MP4	01680-68702	1	Accessory Pouch
MP5	01680-94313	1	Label - Pod and Cable
MP6	01680-94314	1	Label - Certification
MP7	01690-00101	1	Deck
MP8	01690-60101	1	Chassis
MP9	01690-60201	1	Front Panel
MP10	01690-68701	1	Sleeve Assembly
MP11	01690-68702	1	Fascia Assembly (includes the following)
	01680-66506		Power Switch Interface Board

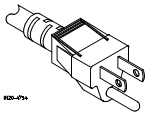
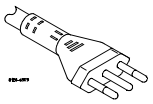
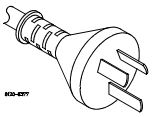
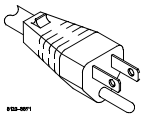
Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
	01690-41901		On/Off Keypad
	01690-44101		Fascia
	01690-61602		On/Off Cable
	0515-1934		M2.5 x 0.45; 6 mm T8 PH (power switch interface board to fascia)
MP12	01690-94302	1	Label - Probe Shroud
MP13	01690-94301	1	ID Label (1690A)
MP13	01690-94304	1	ID Label (1690AD)
MP13	01691-94301	1	ID Label (1691A)
MP13	01691-94302	1	ID Label (1691AD)
MP13	01692-94301	1	ID Label (1692A)
MP13	01692-94302	1	ID Label (1692AD)
MP13	01693-94301	1	ID Label (1693A)
MP13	01693-94302	1	ID Label (1693AD)
MP14	01690-94305	1	Warning Label
MP15	01690-94303	1	Rating Label
MP16	0361-1787	8	Push Rivet (Fan to Chassis)
MP17	0400-0929	4	Snap (accessory pouch to sleeve)
MP18	1400-1254	3	Cable Clip 0.5 in diameter 0.75 in wide PVC (fan cables to chassis, on/off cable to chassis)
MP19	16600-49301	2	Molded Plastic Bumper
MP20	16600-68707	1	Handle Assembly
MP21	5022-1188	1	Front Frame
MP22	5041-9171	2	Side Trim
MP23	5041-9176	1	Top Trim
MP24	54503-25701	2	Hex Nut
MP25	54810-61001	4	Bottom Foot
W1	01680-61609	2	Fan Cable
W2	01690-61601	1	Line Cable Assembly (chassis rear to power supply)
W3	01690-61603	1	Power Sense Cable (power supply to distribution board)
W4	01690-61604	1	Power Supply On/Off Cable (power supply to distribution board)
W5	16715-61601	4	Probe Cable (1690A, AD)
W5	16715-61601	3	Probe Cable (1691A, AD)
W5	16715-61601	2	Probe Cable (1692A, AD)
W5	16715-61601	1	Probe Cable (1693A, AD)

Power Cables and Plug Configurations

This instrument is equipped with a three-wire power cable. The type of power cable plug shipped with the instrument depends on the country of destination.

Plug Type	Cable Part No.	Plug Description	Length (in/cm)	Color	Country
Opt 900 250V 	8120-1703	90°	90/228	Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
Opt 901 250V 	8120-0696	90°	87/221	Mint Gray	Australia, New Zealand
Opt 902 250V 	8120-1692	90°	79/200	Mint Gray	East and West Europe, Saudi Arabia, So. Africa, India (unpolarized in many nations)
Opt 903** 125V 	8120-1521	90°	90/228	Jade Gray	United States, Canada, Mexico, Philippines, Taiwan
Opt 919 250V 	8120-6799	90°	90/228		Israel
Opt 920 250 V 	8120-6871	90°			Argentina
Opt 906 250V 	8120-2296	1959-24507 Type 12 90°	79/200	Mint Gray	Switzerland
Opt 912 250V 	8120-2957	90°	79/200	Mint Gray	Denmark
Opt 917 250V 	8120-4600	90°	79/200		Republic of South Africa India

Plug Type		Cable Part No.	Plug Description	Length (in/cm)	Color	Country
Opt 918 100V		8120-4754	90°	90/230		Japan
Opt 921		8120-6979	90°			Chile
Opt 922		8120-8377	90°			People's Republic of China
Opt 927		8120-8871	90°			Thailand

* Part number shown for plug is industry identifier for plug only. Number shown for cable is Agilent Technologies part number for complete cable including plug.
** These cords are included in the CSA certification approval of the equipment.
E = Earth Ground
L = Line
N = Neutral

8

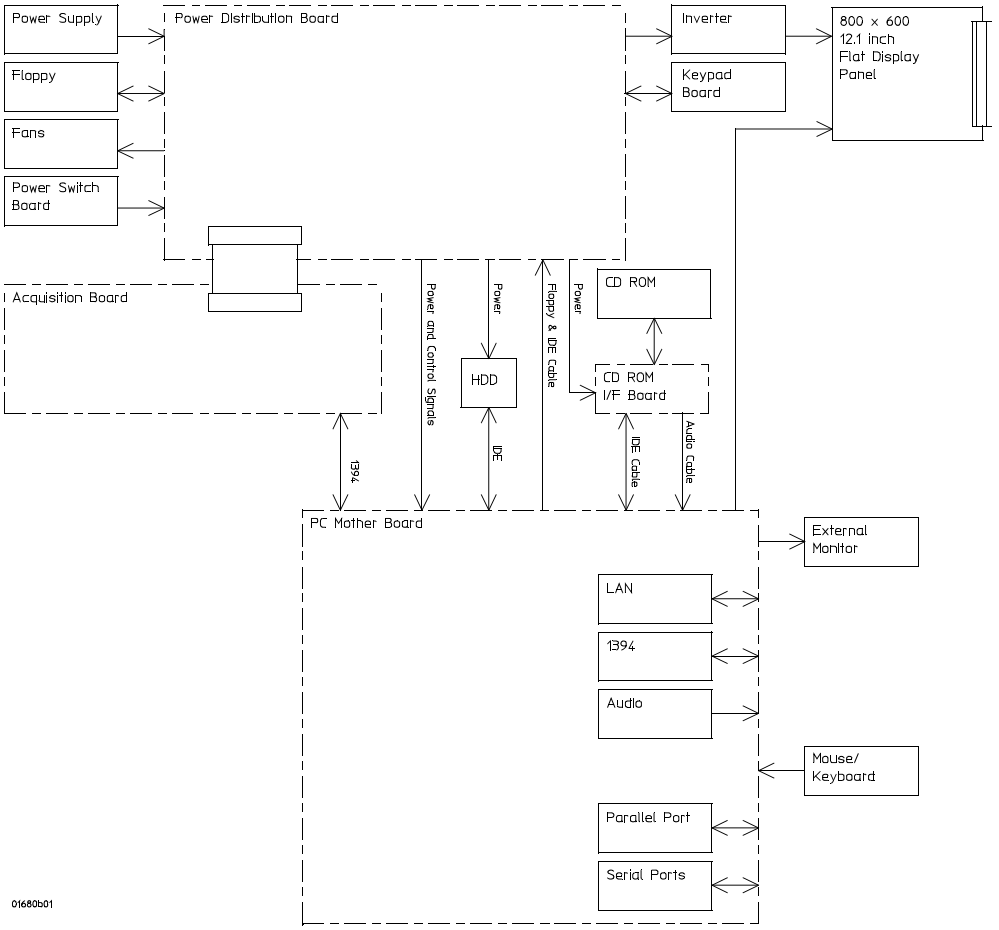
Theory of Operation

This chapter tells the theory of operation for the logic analyzer and describes the self-tests.

The information in this chapter will help you understand how the logic analyzer operates and what the self-tests are testing. This information is not intended for component-level repair.

Block-Level Theory

The block-level theory is divided into two parts: theory for the logic analyzer and theory for the acquisition boards. A block diagram is shown with each theory.



Agilent 1680A,AD-Series Logic Analyzer Block Diagram

Agilent 1680A,AD-series Logic Analyzer Theory

PC Motherboard. The Agilent 1680A,AD-series benchtop analyzer is built around an x86 ATX motherboard. The motherboard serves as the system backplane through PCI slots and IEEE 1394 ports. The hard drive, flexible disk drive, and communications ports are all integrated into the 1680A,AD-series logic analyzer through the PC motherboard. PCI slots are used to house LAN, video, and the IEEE 1394 interface.

PC Software System. The user interface and I/O run on the PC motherboard under Microsoft Windows ® 2000 Professional operating system. This is the primary software system. Windows ® 2000 Professional operating system. This is the primary software system. Windows ® 2000 Professional provides all the graphics drivers needed to create the front panel interface as well as providing all of the software necessary to access the disk drives, to drive printers, and to process input from pointing devices and the keyboard. Standard Windows ® drivers are also used for I/O boards installed in the PCI slots and devices connected to LAN, video, and the IEEE 1394 interface.

Disk Drives. The Agilent 1680A,AD-series logic analyzer contains a 3.5” hard disk drive as well as a 3.5” micro flexible disk drive.

Flat Panel Display. The Agilent 1680A,AD-series logic analyzer includes an active matrix thin flim transistor (AM-TFT) liquid crystal color flat panel display (LCD). The LCD had a resolution of 800 x 600 (SVGA resolution) that measures 12.1 diagonally.

Luminance is software selectable at either 60% luminance or 100% luminance. The display’s luminance is controlled from the user interface by sending commands to the IEEE 1394 processor which in turn sends commands to the front panel microcontroller where luminance is controlled. This board plugs into a PCI slot on the PC motherboard and has a cable that drives the display.

An inverter is used to provide power to the two fluorescent lamps that make up the backlight of the liquid crystal display. The inverter’s output voltage is derived from a +12 V input. The inverter is a separate OEM component that is powered from the power distribution board.

A custom SVGA display board plugs into a PCI slot. The SVGA board drives the flat panel display and can also drive a standard external CRT display.

Networking. Networking is accomplished using an OEM board that plugs into a PCI slot.

Other I/O. The parallel port, audio port, keyboard port, mouse port, serial port, and USB ports are all integrated onto the motherboard.

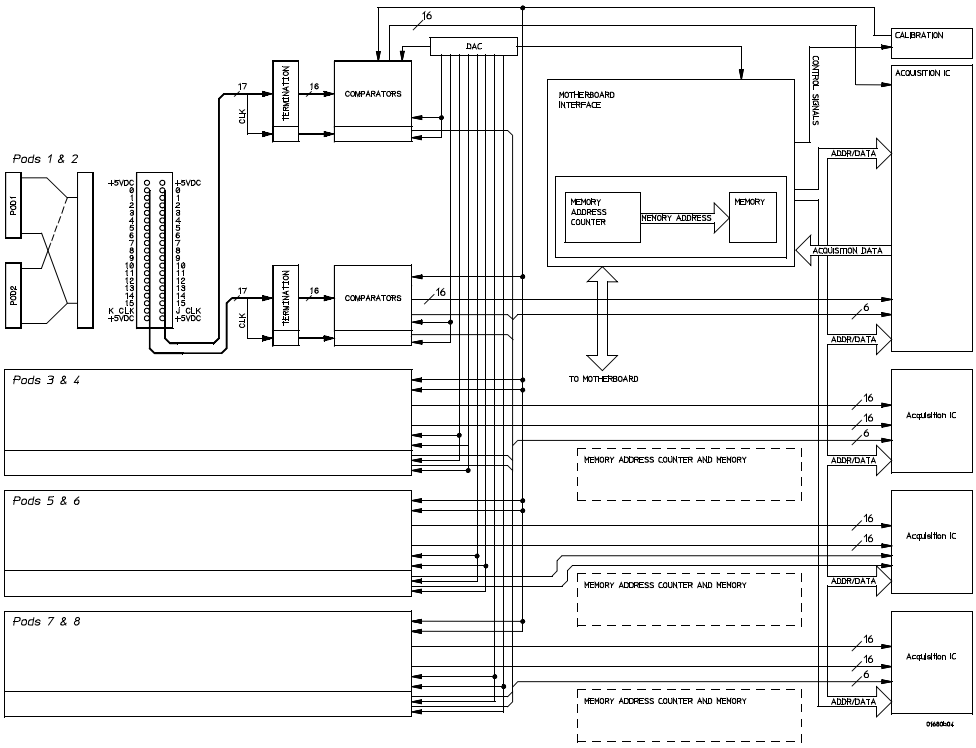
Power Supply

A low voltage power supply provides all the DC voltages needed to operate the logic analyzer. The power supply also provides the +5V VDC voltage to the probe cables to power the logic analyzer accessories and analysis probes.

Unfiltered voltages of +12V, -12V, +5V, -5.2V, +3.4 V and +5V (standby) are supplied to the power distribution board where they are filtered and distributed to other boards and components in the system.

Acquisition Board

Logic Acquisition Board Block Diagram



Probing. The probing system consists of a tip network, a probe cable, and terminations that reside on the analyzer board. Each probe cable is made up of two ribbonized coaxial cables carrying 16 data channels and 1 clock/data channel.

Each channel of the probing system had its own ground. In addition, the pod has a single ground. For applications where many channels are used (greater than three) and signal times are less than 3 ns, individual channel grounds should be used.

The probe tip networks are comprised of a series of resistors (250 Ohm) connected to a parallel combination of a 90 KOhm resistor and an 8.5 pF capacitor. The parallel 90 KOhm and 8.5 pF capacitor along with the glossy cable and terminations form a divide-by Ohm tip resistor is used to buffer (or raise the impendence of) the 8.5 pF capacitor that is in series with the cable capacitance.

Comparators. Two 9-channel comparators interpret the incoming data and clock signals as either high or low, depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparators has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, the operating system software can test all data and clock channel pipelines on the circuit board through the comparator.

Acquisition. Each acquisition circuit is made up of a single acquisition circuit. Each acquisition is a 34-channel state/timing analyzer. One to four acquisition ICs are included on each logic analyzer board for a total of up to 128 data channels and four state clock (pods one through four) in state mode. There are 136 data channels available in timing mode. All of the sequencing, store qualification, pattern/range recognition and event counting functions are performed by the acquisition IC.

Additionally, the acquisition ICs perform master clocking functions. All four state acquisition clocks are sent to the first two acquisition ICs, and the acquisition ICs generate their own sample clocks. When necessary, the acquisition ICs individually perform a clock optimization after the user selects the RUN icon and before data is stored.

Clock optimization involves using programmable delays in the acquisition ICs to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a 100 MHz clock signal to each of the acquisition IPs where they are multiplied by a PLL to obtain the necessary internal clock frequency. For high speed timing acquisition, the master acquisition IC derives the sampling frequency using its PLL and redistributes this sampling clock to the other acquisition ICs.

Acquisition RAM. The acquisition RAM is external to the acquisition IC. The acquisition RAM consists of 9 RAM ICs per acquisition chip. A CPLD, which is initialized by the FPGA, increments the memory addresses while reading or writing to the memory. Memory is read to the FPGA where it is translated and

resent via DMA transactions to an IEEE 1394 Link Layer chip. The Link Layer then transmits the data to a 1394 PHY (physical layer chip) where the data is transmitted over a 1394 cable to the motherboard for processing.

Test and Clock Synchronization Circuit. ECLinPS (ECL in pico seconds) ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification (self-tests). The test patterns are propagated across all data and clock channels and read by the acquisition ICs to verify that the data and clock pipelines are operating correctly.

Clock and Data Threshold. The threshold circuit includes a precision octal DAC. Each of the eight channels of the DAC is individually programmable which allows the user to set the thresholds of the individual pods. The 16 data channels and the clock/data channel of each pod are all set to the same threshold voltage.

Motherboard Interface. The motherboard communications to the acquisition board over an IEEE 1394 interface residing on the acquisition board. Changes to the logic analyzer configuration made in application software are translated into configuration commands and then sent to the acquisition board through this interface. All state and timing functions including storage qualification, sequencing, assigning clocks and qualifiers, RUN and STOP, and thresholds are controlled in the manner.

A microcontroller manages initialization of the acquisition board at power-up, reconfiguring the acquisition board as a result of user input, and managing the IEEE 1394 communication to and from the motherboard.

A field programmable gate array (FPGA) bridges the 1394 interface to the rest of the acquisition board components. It also serves as the memory controller for the acquisition memory.

Memory Address Counters (MACs). Each acquisition IC has a CPLD that is used to provide addresses to the memory ICs that are written during an acquisition. The MACs are also used when uploading data to the GUI. Each CPLD contains three MACs. The MACs are configured serially by the FPGA prior to each acquisition and prior to each data upload. The application is responsible for setting up the proper address by writing to various register in the FPGA, which results in the MACs being serially programmed by the FPGA.

+5 VDC supply. The +5 VDC supply circuit supplies power to active logic analyzer accessories such as analysis probes. Thermistors on the +5 VDC supply lines protect the logic analyzer and the active accessory from overcurrent conditions. When an overcurrent condition is sensed, the thermistors create an open that shuts off the current rom the +5 VDC supply. After the overcurrent condition is resolved the thermistor closes the circuit and makes the supply current available.

Power Distribution Board

The power distribution board connects directly to the power supply and distributes power to the rest of the boards in the system including the motherboard. It also distributes power to the disk drives, fan, and CD-ROM. It has circuity for regulating fan voltage that is temperature dependent as well as detecting when a fan ceases to spin.

The board also converts standard ATX IDE interface signals into those used by notebook flexible disk drives and hard disk drives if needed in the system. The power distribution also distributes various signals between boards such as serial lines and front panel ID signals that connect between the acquisition board and the front panel board.

Front Panel Board

The front panel board contains a microcontroller that is powered from 5V. This particular 5V line comes from a standby rail that is supplied as long as the unit is connected to AC power. The standby rail powers the microcontoller and some core circuitry on the front panel board. The remaining circuitry on the front panel board is powered by the main 5V rail after the supply is turned on by the front panel microcontroller.

The standby power also supplies a small portion of the motherboard circuitry. When the motherboard detects that the power switch has been pressed, it will assert a signal to the microcontroller (via the power distribution board) that tells the front panel microcontroller to turn the main rails of the power supply on or off. After the system's main rails have been powered up, the front panel microcontroller is then free to turn on front panel LED's scan the keypad, and drive control signals to the inverter that cause the display to dim or turn on/off.

The logic analyzer application communicates with the front panel by sending commands to the acquisition microcontroller, via the 1394 bus, which are then transmitted serially by the acquisition microcontroller to the front panel microcontroller. Data is transmitted in the reverse order when the application is polling the front panel.

Agilent 1690A,AD-series Logic Analyzer Theory

Acquisition Board

The Agilent 1690A,AD-series logic analyzers utilize the same acquisition board as the 1680A,AD-series benchtop logic analyzers. The motherboard interface connects directly to the IEEE 1394 port on the host PC.

Power Supply

A low voltage power supply provides all the DC voltages needed to operate the logic analyzer acquisition board. The power supply also provides the +5V VDC voltage to the probe cables to power the logic analyzer accessories and analysis probes.

Unfiltered voltages of +12V, +5V, -5.2V, and +3.4 are supplied to the power distribution board where they are filtered and distributed to other boards and components in the system.

Power Distribution Board

The power distribution board connects directly to the power supply and distributes power to the rest of the system. The power distribution board has circuitry for regulating fan voltage that is temperature dependent as well as detecting when a fan ceases to spin.

Self-Tests Descriptions

The self-tests identify the correct operation of major functional areas in the logic analyzer. The self-tests are not intended for component-level diagnostics.

Three types of tests are performed on the Agilent 1680A,AD- and 1690A,AD-series logic analyzers: the power-up self-tests, the functional performance verification self-tests, and the parametric performance verification tests.

The power-up self-tests are performed when power is applied to the instrument.

The functional performance verification self-tests are run using a separate operating system, the performance verification (PV) operating system.

Parametric performance verification requires the use of external test equipment that generates and monitors test data for the logic analyzer to read. The performance verification procedures in chapter 3 of this service guide make up the parametric performance verification for the logic analyzer. Refer to chapter 3, "Testing Performance," for further information about parametric performance verification.

Power-up Self-Tests (1680A,AD-series)

The power-up self tests on the 1680A,AD-series logic analyzers is performed by the Microsoft Windows ® 2000 Professional operating system. As part of the Windows 2000 Professional power on self test (POST), the presence of all required system components is verified. When the text "Starting Windows . . ." appears, this means required system components have been detected and have passed their individual power-up self-tests.

For more information on the Windows ® 2000 Professional POST, refer to Microsoft on-line(http://www.microsoft.com) and the Microsoft Support Services Knowledge Base (http://search.support.microsoft.com/kb/).

Connectivity Tests (1690A,AD-series)

A Connectivity test routine is done on an Agilent 1690A,AD-series hosted logic analyzer when it is connected to a host PC. A communications test is first done on the hosted logic analyzer when the IEEE 1394 plug and play interface is connected between the host PC and the logic analyzer. After the communications test is successfully completed, an operational accuracy calibration is done on the logic analyzer to test the major subsystems of logic analyzer acquisition and to initialize the acquisition system.

Acquisition Board Self Tests

The acquisition board self tests are available in the Agilent Logic Analyzer application software user interface. These self tests verify the correct operation of the acquisition board in both the Agilent 1680A,AD-series and 1690A,AD-series logic analyzers

Register Test. The Register Test verifies that the registers of each acquisition IC are operating properly. Test patterns are written to each register on each acquisition IC, read, and compared with known values. The registers are reset, and verified that each register has been initialized. Test patterns are then written to ensure the chip address lines are not shorted or opened. Finally test data is written to registers of individual acquisition ICs to ensure each acquisition IC can be selected independently.

Passing the Register Test implies that the acquisition IC registers can store acquisition control data to properly manage the operating of each IC.

Memory Test. The Memory Test verifies that each bit in the acquisition memory IC can be written with a logic “0” and logic “1” through the Serial Access Memory port. Test data is generated using a shifting test register in the acquisition ICs. The serialized test patterns are then sent to the memory port of each acquisition memory IC and stored. The data in the acquisition memory ICs are then downloaded and compared with known values.

Passing the Memory Test implies the acquisition memory can store data written through the memory port. This test along with the Memory Modes Test provides complete testing of the memory ICs.

Comparator Test. The Comparator Test ensures the data signal comparators in the module front end can be set to their maximum and minimum thresholds and that they recognize activity at the signal inputs. A clock signal is routed to a test port on each comparator. The threshold is then set to the minimum value. The comparator output is then read and compared with a known value. The threshold is then set to a maximum value. The comparator output is again read and compared with a known value.

Passing the Comparators Test implies that the front-end comparators are operating properly, can recognize both a logic ì0î and logic ì1î, and can properly send the acquisition data downstream to the acquisition ICs.

Trigger Bus Test. The Trigger Bus Test verifies the trigger resource lines that run between each acquisition IC. The test ensures that the trigger resource lines can be both driven as outputs and read as inputs. The resource registers are written with test patterns, read back, then compared with known values. The resource registers are then written with test patterns, read back from a different acquisition IC, then compared with known values.

Trigger Arm Test. The Trigger Arm Test verifies that the local arm signal can be received by the master acquisition IC on the acquisition board. The test also verifies the global arm signal can be driven by each acquisition IC on a master board and received by all acquisition ICs on the card. The arm lines are asserted and read at the acquisition ICs to ensure each acquisition IC recognizes the signal.

Passing the Trigger Arm Test implies any acquisition IC can arm the card and that all acquisition ICs can recognize the arm signal.

Clock Paths Test. The Clock Paths Test verifies that the system Master, Slave, and Psync clocks are functional between the acquisition ICs. The module is configured to take a simple measurement. Test data is then created at the comparators and an acquisition taken. The resulting data is then downloaded and compared with known values.

Passing the Clock Paths Test implies that all acquisition IC clock lines can be driven by each acquisition IC and can be received by each acquisition IC in the module. Consequently each acquisition IC can reliably acquire data in response to the acquisition clock signal.

Memory Modes Test. The Memory Modes Test verifies the CPU interface can properly manage the acquisition memory unload in full channel, half-channel, count only, and interleaved modes. Test data is written to acquisition memory. Different unload modes are selected, then the data is read and compared with known values.

Passing the Memory Modes Test implies that the data can be reliably read from acquisition memory in full channel, half-channel, count only, and interleaved mode. This test along with the Memory Test provides complete testing of acquisition memory downloading through the 1394 interface.

Calibration Test. The Calibration Test ensures that each acquisition IC in the module can perform an operational accuracy self-calibration. Various self-calibration routines are initiated. The results of each self-calibration routine are then checked to see if the self-calibration was successful or not.

Passing the Calibration Test implies that the module can reliably perform an operation accuracy self-calibration. Consequently the incoming data path is optimized to reduce channel-to-channel skew so the acquisition ICs can reliably capture the incoming data.

Logic Analyzer Self-Tests

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Passing the Register Test implies that the acquisition IC registers can store acquisition control data to properly manage the operating of each IC.

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Passing the Memory Test implies the acquisition memory can store data written through the memory port. This test along with the Memory Modes Test provides complete testing of the memory ICs.

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Passing the Calibration Test implies that the module can reliably perform an operational accuracy self-calibration. Consequently the incoming data path is optimized to reduce channel-to-channel skew so the acquisition ICs can reliably capture the incoming data.

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Manual Part Number

01680-97016

Edition

01680-97003, October 2001
01680-97010, June 2004
01680-97011, August 2004
01680-97014, March 2005
01680-97016, October 2005

Printed in Malaysia

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USA

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