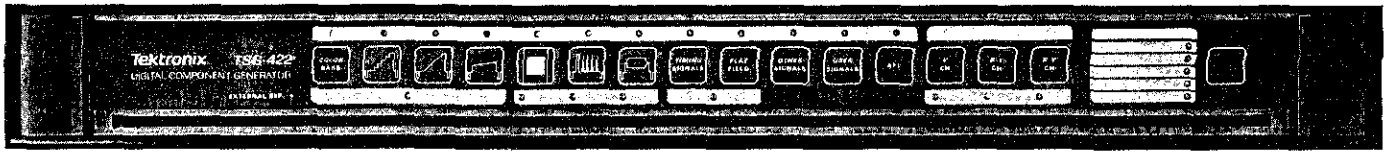
# Digital Component Generator

## TSG-422




*TSG-422 Digital Component Generator.*

### Features

- Conforms to ITU-R BT. 601/656, EBU Tech 3267, and SMPTE 125M, 259M, and RP165
- D1 VTR and Other 4:2:2 Component Digital Equipment Testing and Maintenance
- 10– or 8-Bit Signal Generation
- Parallel Digital Video Test Signal Outputs
- Four Serial Digital Video Outputs (Opt. 1S)
- Separate Y, B-Y, R-Y Clock Outputs
- 525/60 and 625/50 Operation
- NTSC or PAL Black Burst Outputs
- Sync Lock to 525/60 or 625/50

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The TSG-422 Digital Component Generator is a CCIR 601, 4:2:2 format digital test signal generator. The TSG-422 provides all the test signals needed to operate, maintain and evaluate 4:2:2 digital equipment. Analog black burst outputs are provided for equipment synchronization.

**TEST SIGNAL GENERATOR**

The TSG-422 signal generation is 10-Bit in all channels and is clocked at 13.5 MHz for the luminance channel and 6.75 MHz for the color difference channels. Color difference samples are co-sited with the odd numbered luminance samples.

The TSG-422 signal complement contains general purpose signals plus those tailored specifically to the 4:2:2 environment. Test signals included are:

- SMPTE color bars
- Color bars (100% and 75%)
- Pluge
- 5-step
- Ramp
- Limit ramp
- Valid ramp
- Modulated ramp
- Light blue shallow ramp
- Shallow ramp
- Shallow ramp matrix
- Pulse and bar
- Field square wave
- Co-siting verification
- Multipulse
- Multiburst
- Full and reduced amplitude sweeps
- Bowtie timing
- 50% flat field
- Convergence pattern
- Digital/analog blanking markers
- Digital gray
- Super black
- APL: high, low, and bounce

The ramp signal extends 5% below blanking and 5% above peak white to provide indication of clipping. The limit ramp provides signal information to test the maximum dynamic range of the system, levels 4 through 1016 in a 10-Bit system.

Shallow ramp, shallow ramp matrix, and light blue shallow ramp are provided for measurement of quantization noise and the detection of rounding and truncation errors.

The co-siting signal provides a one sample wide, peak white pulse on each horizontal scan line. The luminance channel pulse occurs on an odd sample and is coincident with the like pulses in the color difference channels. This signal is intended to provide an easy means of verifying correct luminance and color difference sample positioning in both the digital and analog domains.

The TSG-422 now provides a new signal for determining the blanking to active picture relationship in a digital television signal, as well as the relative timing between two different digital signals. This signal, the Active Picture Timing Test Signal, provides markers for both digital and analog, vertical and horizontal blanking location.

The digital gray signal sets the luminance channel to word 508 and the color difference channel to word 512. This sets up a high/low sequence on each of the parallel interface lines, thus providing a high frequency signal for testing of the transmission medium.

The TSG-422 also provides facilities for time offsetting the clock and data information. This is useful in verifying receiver performance.

In addition, the frequency of the 27 MHz interface clock may be shifted by 200 Hz in either direction. This provides a means for testing phase lock loops in clock regeneration circuits.

Two separate digital test signal outputs are provided.

Separate outputs of each clock signal are also provided. These outputs are useful in demultiplexing the digital test signal data for conversion to analog for further analysis.

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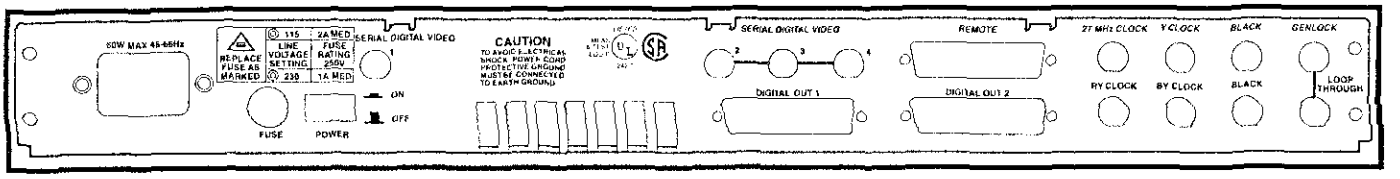


*TSG 422 rear panel with Option 1S Serial Digital Video Output.*

**SERIAL DIGITAL VIDEO INTERFACE**

The serial digital video option for the TSG-422 provides four serial outputs. These are user configurable for either black or test signal. If configured for test signal, these outputs follow the front panel test signal selection. Signal specifications meet all related digital video and audio standards.

An error detection (EDH) signal is located in the ancillary data area of line 9 (525 systems) or line 5 (625 systems). This signal contains two cyclic redundancy code (CRC) calculations, one for the digital data in each field and one for the digital data in the active picture of each field. Comparison of the CRC values with those calculated in the receiver will provide a real time, on-line error rate measurement.

Three special flat field (SDI check field) signals are provided for serial digital interface testing. These valid component digital signals are designed to test receiver serial equalization and clock recovery.

Four channels of AES/EBU digital audio are embedded in the serial digital video. Internal DIP switch selection of frequency, silence, or off is provided for each channel pair. In addition, the status bit may be set to indicate emphasis on or off for checking of devices with automatic detection and switching of audio de-emphasis. This feature provides functionality checking only as there is no pre-emphasis of the embedded audio at any time.

Serial digital video output is available as an option for new generators and as a field upgrade kit for existing TSG-422 generators.

The TSG-422 now provides a new signal for determining the blanking to active picture relationship in a digital television signal as well as the relative timing between two different digital signals. This signal, the Active Picture Timing Test Signal, provides markers for both digital and analog, vertical and horizontal blanking location (see Figure 1).

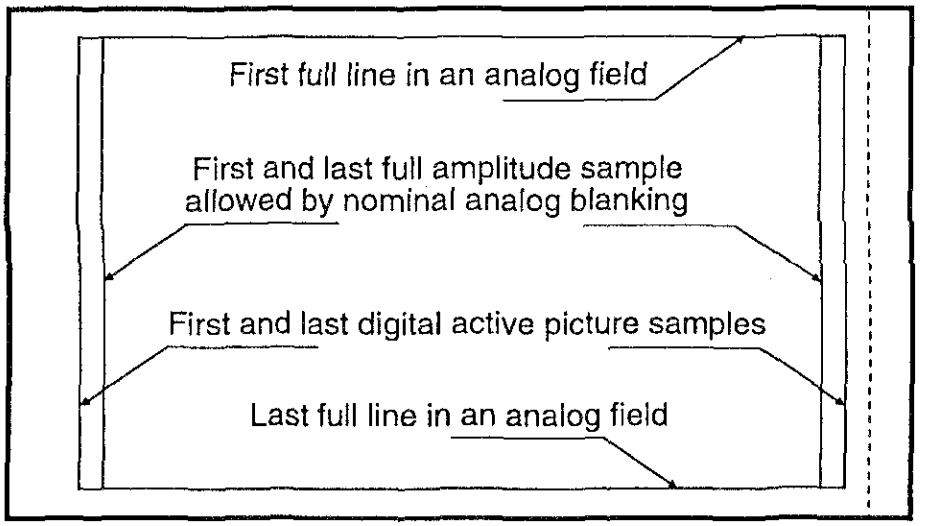


*Figure 1. Picture monitor display of the Active Picture Timing Test Signal.*

## Characteristics

**TEST SIGNAL GENERATOR**

**Sampling Frequency –**
Luminance Channel: 13.5 MHz.
Color Difference Channels: 6.75 MHz.

**Digital Coding –**
*10-Bit or 8-Bit linear PCM in all channels.*

**Video to Quantization Level Relationships –**
Luminance Channel: 877 levels with black at level 64 and white at level 940.
Color Difference Channels: 897 levels centered around level 512.

**PARALLEL DIGITAL INTERFACE**

**Output Format** – Balanced ECL (10 K series); 10 data pairs, 1 clock pair, system ground, chassis ground.

**Interface Clock** – 27.0 MHz.

**SERIAL DIGITAL VIDEO INTERFACE**

**Digital Format –**
CCIR 601 Component; 525/60 or 625/50; 8-Bit or 10-Bit Data; Scrambled NRZI.

**Bit Rate** – 270 Mb/s.

**Ancillary Data –**
Error Detection: Active Picture and Full Field CRC Words; Located on Line 9 for 525/60 and Line 5 for 625/50.

**Digital Data –**
Amplitude: 800 mV ± 10% into 75 Ω.
Rise and Fall Times: 1 ns ± 250 ps (20% to 80% Amplitude Points).
*Jitter: <±250 ps (measured over a one* horizontal line period).
DC Offset: 0 ± 0.5 V.

**Outputs –**
Number of/Connector: 4/BNC.
Impedance: 75 Ω.
Return Loss: >15 dB, 5 to 270 MHz.

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**EMBEDDED AUDIO**
**Sampling Frequency** – 48 kHz, locked to video.
**Digital Coding** – 20 bits linear PCM, two compliment coding.
**Number of Channels** – 4
**Frequency** – 1 kHz, 800 Hz, or silence.
**Level** – 20 dB below peak.

**CLOCK OUTPUTS**
**Luminance Channel** – 13.5 MHz.
**Color Difference Channels** – 6.75 MHz.
**Connector** – BNC.

**SYNC GENERATOR**
**Line and Field Rates** – 525/60 or 625/50 (user selectable).
**Black Burst** –
2 Outputs: NTSC in 525/60 mode PAL in 625/50 mode.
**Blanking Width** –
NTSC: 10.9 µs.
PAL: 12.0 µs.
**Genlock** – Loop-through input; Locks to NTSC, PAL, SECAM, or component luminance.
**Genlock Timing Range** – 8 µs of advance and delay.

**POWER SOURCE**
**Mains Ranges** –
Voltage: 90 to 132, 180 to 250 V AC.
Frequency: 48 to 66 Hz.
**Power Consumption** –
60 W typical; 80 W max.

**ENVIRONMENTAL**
**Temperature** –
Operating: 0° to + 50°C.
Nonoperating: –40° to + 65°C.

***CERTIFICATIONS***
**EMC** – Certified to the EMC Directive 89/336/EEC.
**Safety** – Approved to: UL1244, CAN/CSA-C22.2 No.231.
Complies with: HD401 S1, IEC 348.

**PHYSICAL CHARACTERISTICS**

| Dimensions | mm | in. |
|---|---|---|
| Height | 44 | 1.734 |
| Width | 483 | 19 |
| Depth | 561 | 22.1 |
| **Weight** | **kg** | **lb.** |
| Net | 6.14 | 13.5 |
| Shipping | 10.41 | 22.9 |

## ORDERING INFORMATION

*For pricing information contact your local Tektronix representative.*

**TSG-422**
Digital Component Generator.
**Opt. 1S** – Adds Serial Digital Video Outputs.
**TVGF03** – Signal Memory Kit to replace 8-Bit signals with 10-Bit signals (Serial number B010253 and below).
**TVGF1SB** – Kit to add Serial Digital Video Outputs to a TSG-422 Generator.

**MEASUREMENT SERVICE OPTIONS**
**Opt. C3** – Three years of Calibration Services.
**Opt. C5** – Five years of Calibration Services.
**Opt. D3** – Test Data (requires Opt. C3).
**Opt. D5** – Test Data (requires Opt. C5).
**Opt. R3** – Repair warranty extended to cover three years.
**Opt. R5** – Repair warranty extended to cover five years.

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