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INSTRUCTION MANUAL

MODEL 802
50 MHz PULSE GENERATOR

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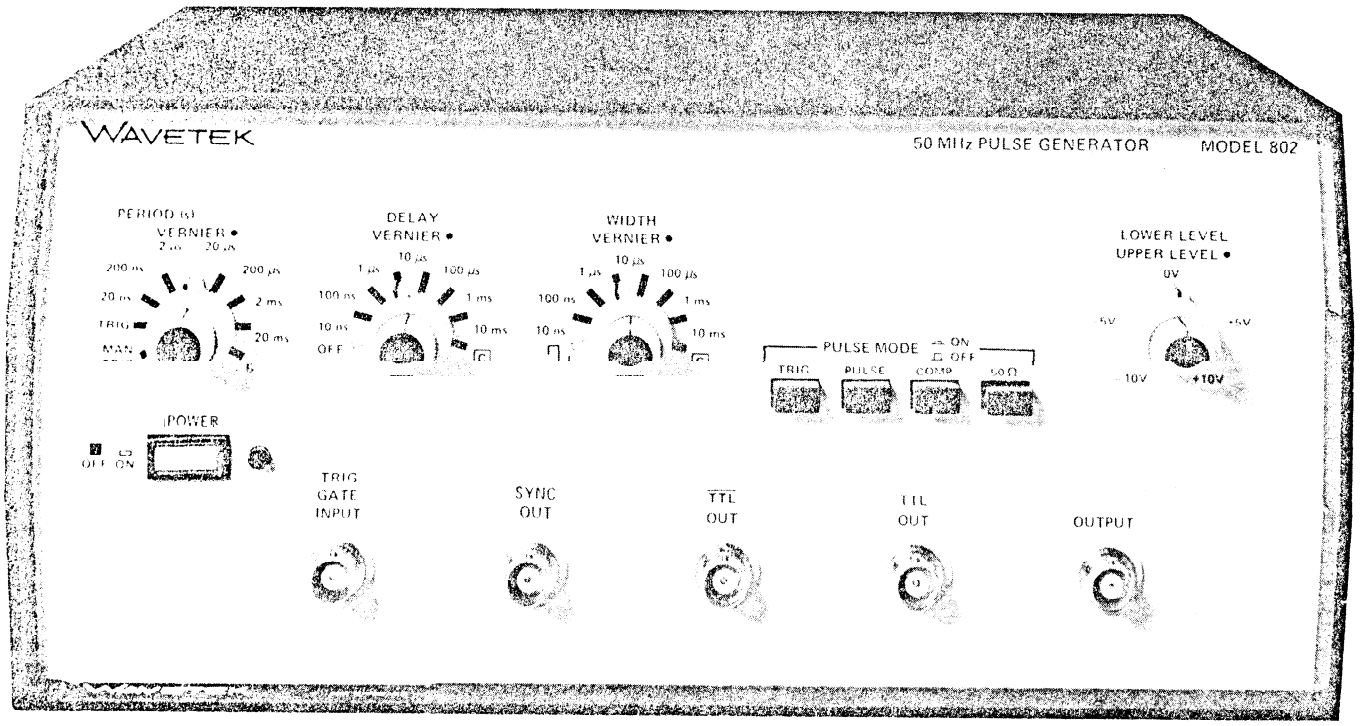


Figure i. Model 802 50 MHz Pulse Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 802

The Model 802 is a 50 MHz **general purpose laboratory** pulse generator. The instrument gives you full control **in primary** pulse triggering and shaping plus simultaneous TTL, $\overline{\text{TTL}}$ **and** sync pulses. The primary pulse output has control-**lability** in rate, width, delay, upper level, lower level and a choice of positive, negative or complementary outputs. The TTL and $\overline{\text{TTL}}$ are of fixed levels and rise times that are standard for use with compatible devices. The primary pulse has rise and fall times of 5 ns or less.

The output is ±10 volts with a 50Ω termination. Upper and lower pulse levels are fully adjustable through ±10 volts, a 20 volt window. Termination may be internal, at the load or both.

Single pulses or pulse pairs may be triggered; pulse width may be trigger controlled; continuous pulses may be gated for a 'burst' output.

'1.2 SPECIFICATIONS

1.2.1 Versatility

Four Simultaneous Pulse Outputs
Fixed TTL level sync, TTL and $\overline{\text{TTL}}$ outputs, and variable amplitude output pulses are available **over a** 5 Hz (200 ms) to 50 MHz (20 ns) frequency range.

For optimum pulse characteristics from the variable amplitude pulse output, an internal 50Ω load can be selected via a front panel control.

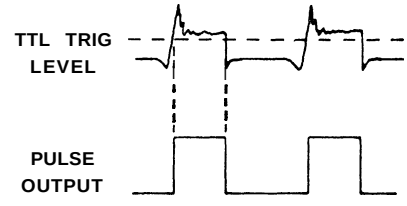
Operational Modes
Continuous: Generator oscillates continuously at selected frequency.

Triggered: Generator quiescent until triggered by external TTL pulse or front panel control, then generates one pulse.

Gated: Generator oscillates at the period rate selected by the front panel control when gate input is high. Generator quiescent when input is low. First cycle is synchronous with rising edge of gating signal.

Double Pulse: Same as continuous, triggered and gated, except two pulses for each period. Time to second pulse is controlled by delay control. Double pulse at all outputs except sync.

External Width: External signal at trigger input determines output pulse width and period as shown.



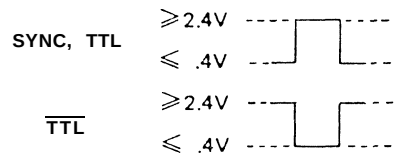
1.2.2 Pulse Outputs

Variable Amplitude Pulse

SOURCE	LOAD	DYNAMIC RANGE	AMPLITUDE MAXIMUM	AMPLITUDE MINIMUM
50Ω	50Ω	+5V / −5V	5V	.5V
1 kΩ OR 50Ω	50Ω / ≥1 kΩ	+10V / −10V	10V	1V

Upper and lower pulse levels are independently adjustable. Pulse dynamic range is ±10V when load is 50Ω terminated and source is not (internal 50Ω off) or vice versa. Maximum pulse amplitude is 1OV; minimum is **1V.** Dynamic range and pulse amplitude are decreased by a factor of 2 when source and load are 50Ω terminated. Overshoot and ringing are less than ±(5% of amplitude setting +IOO mV) when terminated into 50Ω at both load and source. Transition times are less than 5 ns.

Sync, TTL and $\overline{\text{TTL}}$ Pulses
Sync pulse levels from 50Ω; TTL and $\overline{\text{TTL}}$ pulse levels into 50Ω termination.



Transition times less than 7 ns into 50Ω termination.

Normal/Complement Control
Normal pulse or its complement is selected. The normally quiescent and active levels are reversed in complement format. This control affects all outputs except sync pulse.

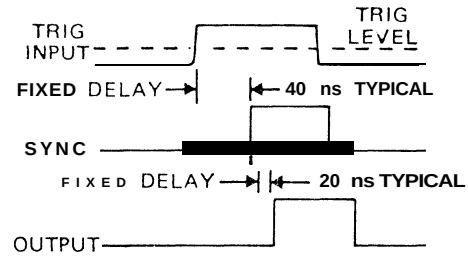
7.2.3 Time Domain

Period
Period range is from less than 20 ns to greater than 200 ms in 7 overlapping ranges. Period jitter is less than ±0.1% plus **50** picoseconds.

Width
Width range is from less than 10 ns to 10 ms in 6 overlapping ranges. Maximum duty cycle is 70% for periods to 200 ns, decreasing to 50% for 20 ns periods. Width selector switch also has a square wave detent and a customer-specified detent.." duty cycle is 50 ±4% to 2 μs period, changing to 50 ±15% at 20 ns period. Width jitter is less than ±0.1% plus 50 picoseconds. Sync pulse duty cycle is 50 ±4% of pulse period to 2 μs period, changing to 50 ±15% at 20 ns period except in trigger and external width modes, in which case it is determined by the trigger signal.

Delay
Pulse occurence can be delayed from less than 10 ns to 10 ms with respect to the sync pulse (not including fixed delay). Delay selector switch also has a customer-specified detent.* Maximum delay duty cycle is 70% for periods to 200 ns, decreasing to 30% for 20 ns periods.

Delay jitter is less than ±0.1% plus 50 picoseconds. Fixed delay is as shown.



1.2.4 Input Characteristics

External Trigger
The circuit receiving the external trigger is TTL compatible. Triggering level is fixed at approximately 1.4V. Input impedance is greater than 500Ω shunted by approximately 33 pF. Triggering and gating occurs on the rising edge of the input signal.

1.2.5 General

Environmental
Specifications apply at 25°C ±5°C after 30 minutes warm-up. Instrument will operate from 0°C to 50°C.

Dimensions
28.8 cm (11.4 in.) wide; 10.2 cm (4 in.) high; 29 cm (11.4 in.) deep.

Weight
4.0 kg (8.9 lb) net; 5.4 kg (12 lb) shipping.

Power
108 to **132V or 216** to **250V; 50** to 400 Hz; 40 watts nominal.

*Customer-installed capacitor determines detent range.

SECTION 2
INSTALLATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc., If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc. between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

*Unless **otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 108 to 126 Vac line supply and with a** 0.5 **amp fuse.***

Conversion to other input voltages requires a change in rear panel fuse-holder voltage card position and fuse according to the following table and procedure.

Card Position	Input Vac	Fuse (Slow Blow, 3 AG)
100	90 to 105	**0.5** amp
120	108 to 126	**0.5** amp
220	198 to 231	***0.25*** amp
240	216 to 250	0.25 amp

1. Open fuse holder cover door and rotate FUSE PULL to left to remove the fuse.

2. Select operating voltage by orienting the printed circuit board to position the desired voltage on the top left side. Push the board firmly into its module slot.

3. Rotate the FUSE PULL back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

Use 3 foot RG58U 50Ω shielded cables equipped with female BNC connectors to distribute input and output signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECK

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A 2 channel oscilloscope and 50Ω coax cable are needed for this procedure (see figure 2-l).

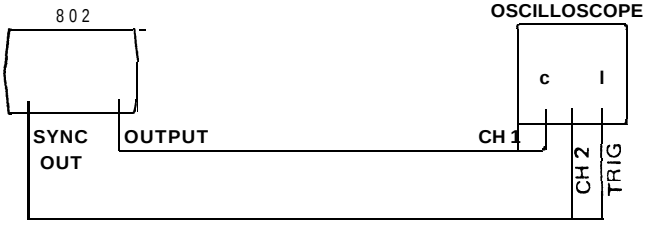


Figure 2-1. Initial Setup

Preset the pulse generator controls by setting the following switches to their white mark:

PERIOD/RATE
DELAY
WIDTH

Set the PULSE MODE switches OFF except set INT 50Ω ON.

Set the foilowing controls to 12 o'clock:

PERIOD/RATE VERNIER
DELAY VERNIER
WIDTH VERNIER
LOWER LEVEL
UPPER LEVEL

Perform the steps in table 2-1. Only approximate values are required to verify operation.

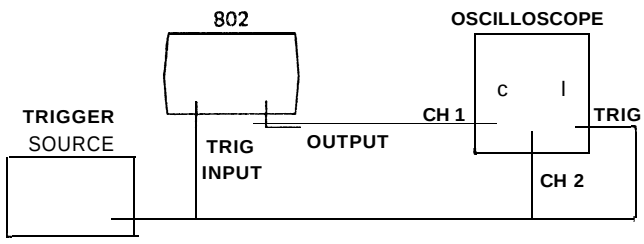


Figure 2-2. Second Setup

Table 2-1. **Performance Checkout**

Step	Control	**Position/Operation**	**Observation**
1	POWER	**ON**	CH 1: A near 0 volt dc level. (LEVEL control is not calibrated.) CH 2: Approximately 2.5 volt pulses.
2	LOWER LEVEL	Rotate ccw	Pulse base drops 1OV.
3	UPPER LEVEL	Rotate ccw	Pulse upper level drops 1OV.
4	UPPER LEVEL_	Rotate cw. Make observation; then reposition for good display	Pulse rises 10V, then rises 1OV more while pulling the base up 1OV. Base rises to OV.
5	COMP	ON then OFF	Set scope for one or two cycles. Observe the switching of duty time from first half cycle to second half cycle.
6	WIDTH	Rotate ccw, then to 10 μs I 100 μs	Pulse width changes. (Use scope X 10 magnification to see narrow widths.)
7	WIDTH VERNIER	Rotate ccw, then to 12 o'clock	Pulse width decreases, then increases.
8	DELAY	Rotate cw to 10 μs I 100 μs	Pulse delay changes within cycle time.
9	DELAY VERNIER	Rotate ccw, then cw	Pulse delay moves to left, then right.
10	PERIOD/RATE VERNIER	Rotate cw, then to 12 o'clock	Period increases, then decreases.
11	DBL PULSE	ON	Two pulses instead of one.
12	DELAY VERNIER	Rotate ccw, then cw, but maintain double pulse	Pulse pairs move closer, then further apart.
13	WIDTH VERNIER	Rotate ccw, then to 12 o'clock, but maintain double pulse	Pulse width of each pulse of pulse pair decreases, then increases.
14	OUTPUT	Remove cable; place on TTL connector	TTL double pulse output.
15	TTL OUT	Remove cable; place on $\overline{\text{TTL}}$ connector	$\overline{\text{TTL}}$ double pulse output complement of previous output.

Table 2-l. Performance Checkout (Continued)

Step	Control	Position/Operation	
16		Change to setup in figure 2-2; trigger with a 10kHz signal; adjust scope for best display	One pulse on **CH** 2; set of pulses on CH 1.
17	**WIDTH**	Rotate to ⊓⊔	One pulse on CH 1; one pulse on CH 2.
18	**MAN TRIG**	ON	Repeated operation makes pulse pair observable.

SECTION 3
OPERATION

3.1 CONTROLS AND CONNECTORS

The generator controls and connections are shown in figure 3-1 and keyed to the following descriptions.

1. PERIOD/RATE **Switch –** Selects one of seven ranges of pulse period calibrated in seconds and hertz. The TRIG detent holds the output at the inactive level until a TTL level trigger signal is applied at the TRIG GATE INPUT BNC. On the input rising edge, one pulse, or one double pulse, is output. The MAN TRIG detent is as the TRIG detent, except pressing the MAN TRIG switch generates the output.

   NOTE
   For continuous mode operation, low input or 50Ω termination to the TRIG GATE INPUT BNC must be removed.

   VERNIER Control – Varies the pulse period within the range selected by the outer knob. Clockwise increases the pulse period and decreases frequency.

2. **DE LAY Switch –** Selects one of seven ranges of pulse delay or time-to-second-pulse of double pulses, depending on DBL PULSE switch setting. **OFF** position of DELAY switch ensures minimum delay. The detent marked "C" is for customer selected range.

   VERNIER Control – Varies the delay time within the range selected by the outer knob. Clockwise increases the delay.

3. **WIDTH Switch –** Selects one of seven ranges of pulse width or an approximate 50% duty cycle. The detent marked "C" is for customer selected range.

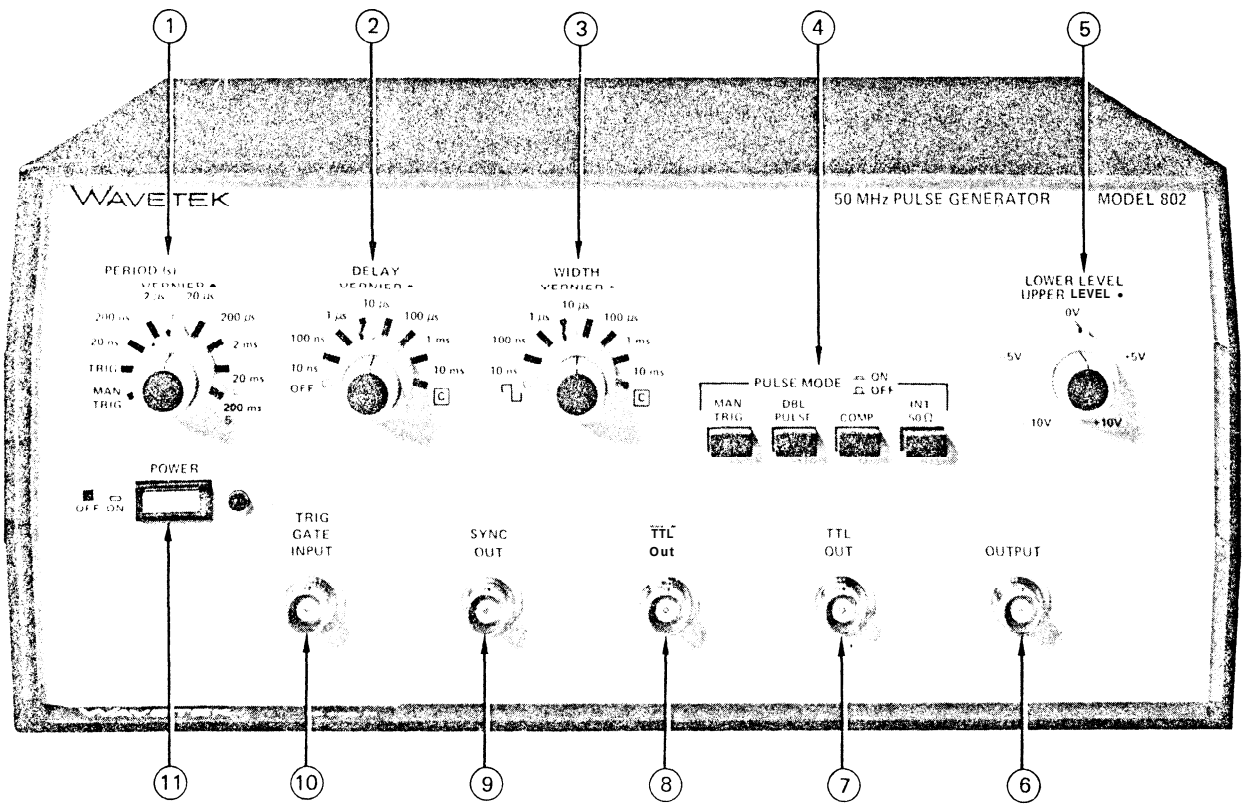


Figure 3-1. **Controls and Connections**

VERNIER **Control** – Varies the pulse width within the range selected by the outer knob except in ⎍.

(4) MAN TRIG **Switch** – Triggers the generator one time when pressed. Output depends on the mode selected.

DBL PULSE Switch – When ON, a double pulse occurs in each period. Time to leading edge of second pulse is controlled by the DE LAY setting. When OFF, one pulse occurs in each period.

COMP **Switch** – **Selects** a normal pulse when OFF or **its** complement when ON, which swaps the active and quiescent levels. Affects all outputs, except SYNC.

INT 50Ω **Switch** – When ON, the output current source is 50Ω terminated internally. When OFF, the current source has greater than 1 kΩ impedance.

(5) LOWER LEVEL **Control** – Outer knob sets the **lower level** of the OUTPUT pulse, which may be varied from -10 to +10 volts into a single 50Ω termination or -5 to +5 volts into a double 50Ω termination. Maximum pulse heights are 10 and 5 volts, r espectively.

UPPER LEVEL **Control** – Inner knob sets the upper level of the OUTPUT pulse. Upper level range is identical to that stated for the lower level.

(6) OUTPUT **Connector** – The main output of the generator. Pulses from this output may be controlled in **level as well as frequency and width.**

(7) **TTL OUT Connector** – An output with a transistor-transistor-logic **level pulse whose occurrence and** duration at-e controllable. **Normal pulselevel is <0.4V quiescent, > 2.4V active** into a 50Ω termination. **Levels are reversed for the complement pulse.**

(8) $\overline{\text{TTL}}$ **OUT Connector** – An output like the TTL output (7) except **active and quiescent** levels are reversed.

(9) **SYNC OUT Connector** – A TTL level output from a 50Ω source. Square wave in all modes except external width and external trigger modes, in which pulse width is determined by trigger pulse width.

(10) **TRIG GATE INPUT Connector** – Accepts an external TTL level signal to trigger or gate the generator. Triggers on rising edge of input. Gates off when level is at a TTL low level.

(11) **POWER Switch** – Pulse generator on/off switch features red power-on indicator light and black/white changing switch surface for off/on indication.

3.2 NOTES ON OPERATION

3.2.1 Modes

The following modes of operation are available and selectable as described herein.

Continuous – For a continuous stream of pulses, the PERIOD switch must be in any position except TRIG or MAN TRIG and the TRIG GATE INPUT BNC must be free of input signals and 50Ω terminations.

Triggered – For a pulse, or pulse pair, triggered by an external signal, the PERIOD switch must be set to TRIG and a TTL level square pulse must be present at the TRIG GATE INPUT. Triggering occurs on the trigger pulse rising edge.

Manually Triggered – For a pulse, or pulse pair, triggered by the MAN TRIG switch, the PERIOD switch must be set to MAN TRIG.

Gated – For continuous pulses for the duration of a gate signal, the PERIOD switch must be in any position except TRIG or MAN TRIG and a TTL level square pulse must be input to the TRIG GATE INPUT BNC. For manual gating, place a 50Ω termination on the TRIG GATE INPUT BNC to disable the generator output. Push the MAN TRIG switch to gate an output.

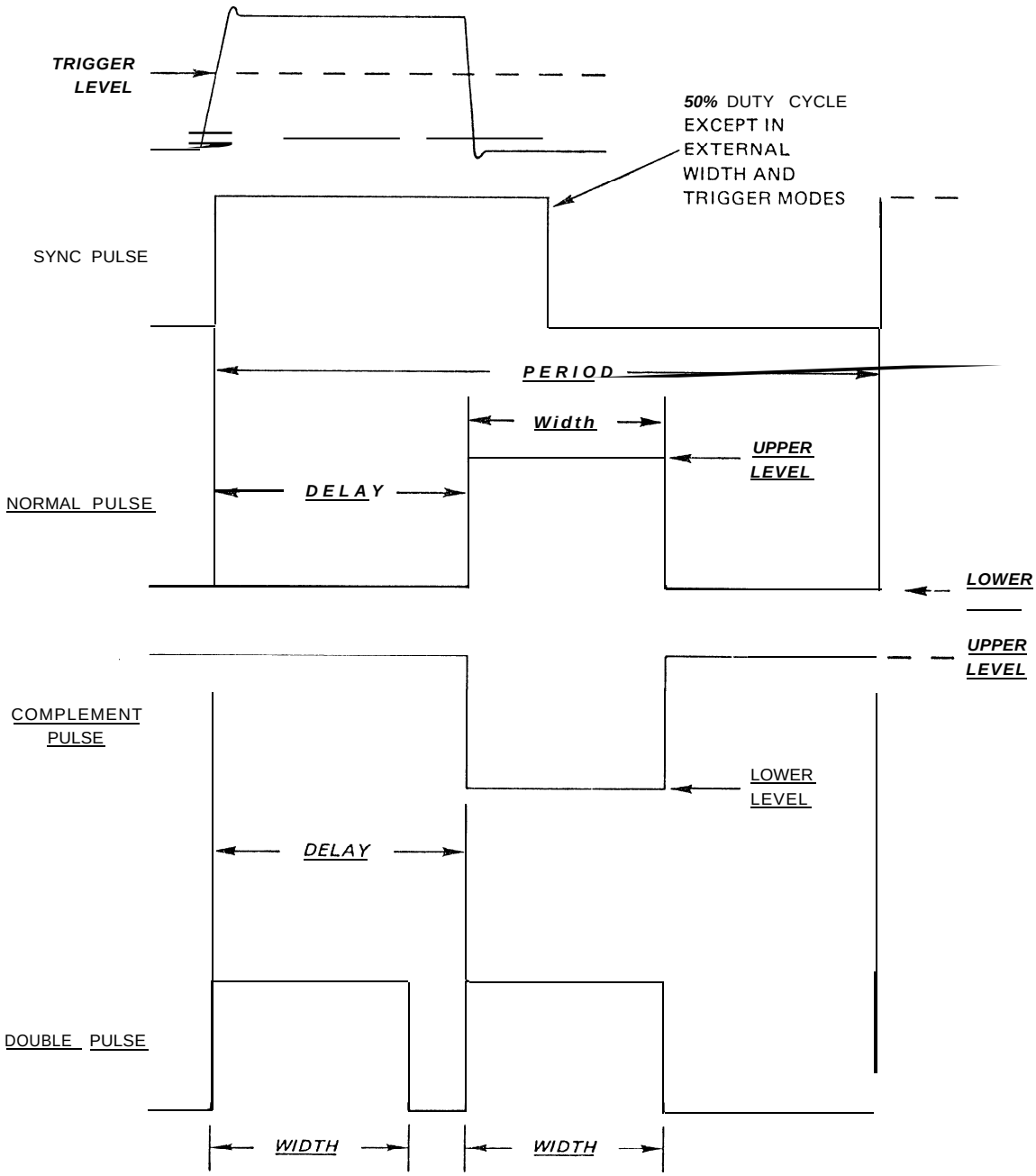
External Width – For pulses whose widths are determined by an external signal, the PERIOD switch must be set to TRIG and the WIDTH switch must be set to ⎍.

3.2.2 White Marks

When first becoming familiar with the 802, the white mark settings are handy. The white mark settings for the front panel switches will always give a 50 to 500 kHz sync signal when power is on. The same settings will give 50% duty cycle TTL, $\overline{\text{TTL}}$ and output pulses; the LOWER LEVEL/ UPPER LEVEL control may need adjusting to observe the output on an oscilloscope, Once the output is observed, each control can be adjusted and observed until the desired result is obtained.

3.2.3 Pulse Width and Delay

Narrow duty cycle pulses require a normal output (COMP OFF) while greater than 70% duty cycle pulses require the COMP ON setting to allow the width circuitry sufficient recovery time. When using DELAY time, ensure that delay ⩽ 70% of PERIOD and width ⩽ 70% of PERIOD.



NOTE: Underline Indicates a front panel con trolled parameter.

Figure 3-2. Pulse Parameters

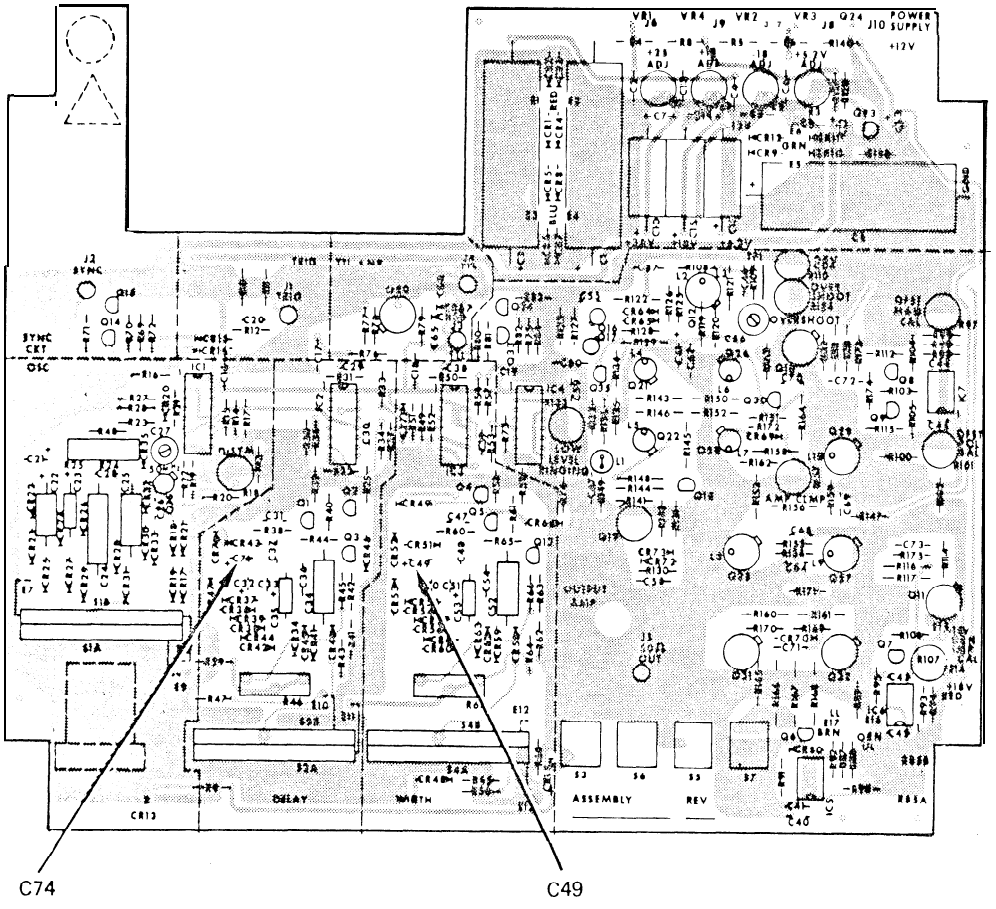


Figure 3-3. Placement of Customer Option Capacitors

The ⎍ width setting gives a 50% duty cycle in continuous mode, when TRIG or MAN TRIG is selected on the PERIOD switch, the pulse width is determined by the trigger signal width. This is external width mode of operation.

Table 3-1. Capacitance and Ranqe

Delay or Width Range	Capacitance
10 ns · 100 ns	None
100 ns - 1 μs	2000 pF
1 μs -10 μs	0.02 μF
10 μs - 100 μs	0.2 μF
0.1 ms · I ms	2.0 μF
1 ms- 10 ms	20 μF
10 ms - 100 ms	200 μF
0.1s · 1s	2000 μF

The unmarked detent on the DELAY switch and WIDTH switch can be any desired range by placing appropriate capacitors on the circuit board, as shown in figure 3-3. Refer to table 3-I for typical capacitance and range.

3.2.4 Output Terminations

Only 50Ω RG58U cables should be used to connect the 802 to the circuit under test. Either the INT 50Ω should be ON or a 50Ω 2W load should be used at the circuit end of the cable. For best pulse fidelity, a 50Ω load at both the source and the load is required.

As shown in figure 3-4, the combinations of load and source impedances determine the output pulse amplitude range

SOURCE	LOAD	DYNAMIC RANGE	AMPLITUDE MAXIMUM	AMPLITUDE MINIMUM
50Ω	50Ω	+5V / −5V	5V	.5V
* 1 kΩ OR 50Ω | ≥1 kΩ	50Ω	+10V / -10V	10V	1V

*1 kΩ is the unterminated source impedance of the OUTPUT.

Figure 3-4. Load and Source Terminations

and the dynamic range. As shown, when a greater than 5V pulse is desired, only one 50Ω termination can be used, and the placement of the termination can optimize the pulse purity. In this case, the capacitance of the circuit being driven must be considered. For capacitive loads greater than 20 pF, reflections on the line are most effectively absorbed by the 50Ω termination at the 802 (INT 50Ω switch ON). For capacitive loads less than 20 pF, the 50Ω termination should be placed at the load side of the line. When a less than 5V pulse is required, a 50Ω termination at each end of the line is recommended for optimum pulse purity.

The 50Ω terminations should always be used on the SYNC, TTL and TTL outputs.

3.2.5 Duty Cycle

Always use the iowest range possible for both delay and width functions. This will reduce the recovery time of the circuit one-shots and extend the maximum duty cycle of the 802 to its fullest capability.

3.2.6 Output Mixing

By triggering a second 802 from the sync output of the first 802 and then mixing their outputs **in a common load, three** level signals can be created, as shown in figure 3-5.

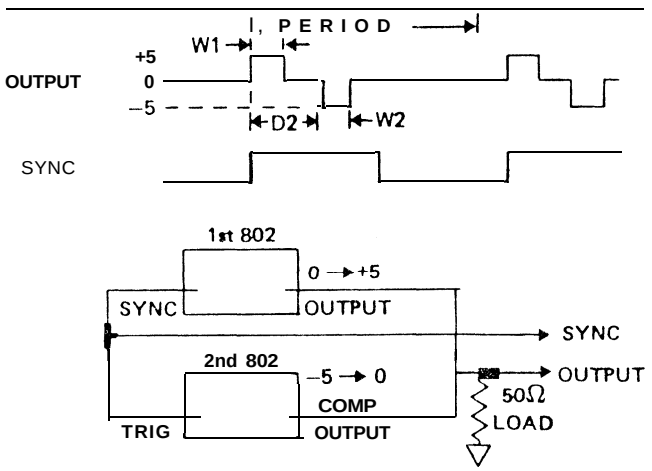


Figure 3-5. Output Mixing

3.2.7 Precise Output Levels

Many times when testing a circuit, it is desirable to lock the output of the generator at either the high or low level. A precise measurement of this level may then be obtained using a DVM.

To lock the output at high or low level, select EXT TRIG and ⊓⊔ with no TRIG GATE INPUT. Use the COMP ON/OFF switch to select high and low level outputs.

3.2.8 Fixed Delay

A fixed delay of 20 ns has been incorporated within the 802 to ensure that the leading edge is visible on the scope. If this delay is not desired, simply increase the length of the sync cable coax at the rate of 1.5 ns/ft to obtain the desired result.

3.2.9 Two Phase Clocking

If a secondary 802 is triggered by the sync out from the primary 802, a two phase nonoverlapped clock source can be obtained as shown in figure 3-6.

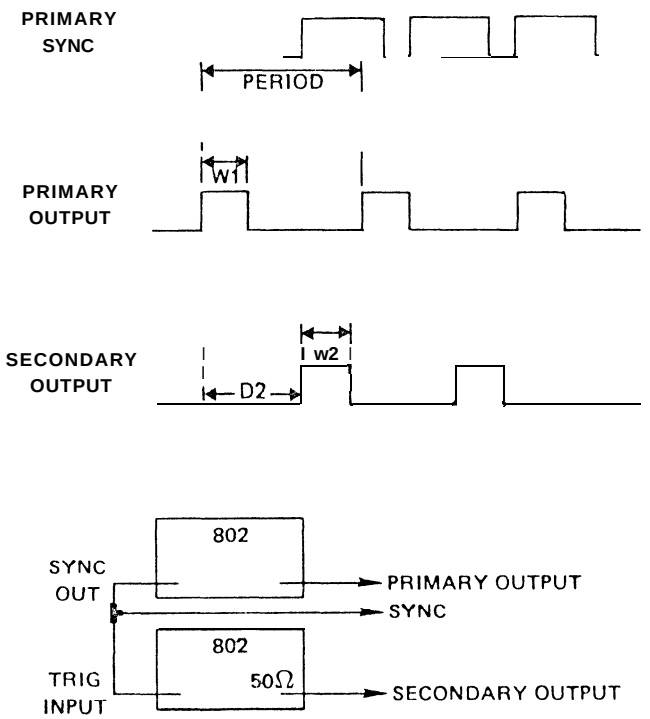


Figure 3-6. Two Phase Clock Generation

3.2.10 Rise Time Measurements

When measuring rise time in a linear device under test, the error induced by the rise time of the testing system must be considered. **For example,** when observing the **802 rise titne** on an oscilloscope, **802** rise time is

$$t^2_{observed} = t^2_{scope} + t^2_{802}$$

or

$$t_{802} = \sqrt{t^2_{observed} - t^2_{scope}}$$

That is, the observed **rise** time **must** be **corrected for by the** inherent oscilloscope rise time to determine **the actual** 802 rise time. Extending the method to include a circuit under test will determine circuit under test rise time:

$$t^2_{observed} = t^2_{802} + t^2_{scope} + Lt.$$

or

$$t_{c.u.t.} = \sqrt{t^2_{observed} - t^2_{802} - t^2_{scope}}$$

3.3 OPERATION

In the following descriptions of operation, observe the pulse on an oscilloscope. In continuous mode, trigger oscilloscope on SYNC **OUT.** In all other modes, trigger on the trigger signal. (See figure 3-2 for pulse parameters.)

Observe the following constraints:

Delay ⩽ 70% of period.
Width ⩽ 70% of period.

3.3.1 Continuous Pulses

Set the controls (and connectors) as follows:

Control	Operation
TRIG GATE INPUT Connector	No signal present
INT 50Ω Switch	ON
PERIOD Switch	Desired range setting
Other Controls	Set as desired

3.3.2 Wide Duty Cycle Pulses

For wider pulses than those that can be normally obtained, set up for a pulse with the complemented width, then press the **COMP** pulse switch ON. For example, if a 95 ns pulse with a 125 ns repetition rate is desired:

$$125\,ns - 95\,ns = 30\,ns$$

Set up for a 30 ns pulse, then press the COMP switch **ON.** (See figure 3-7.)

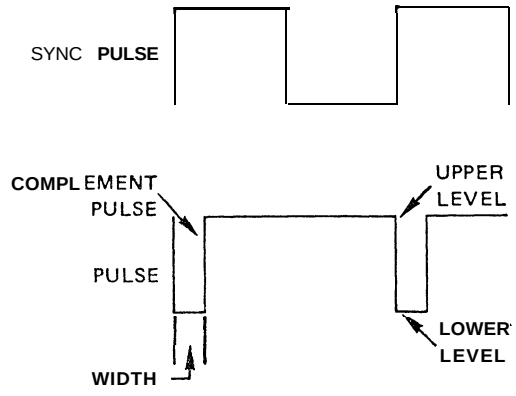


Figure 3-7. Greater Than 70% Duty Cycle Pulse

3.3.3 Externally Triqgered Pulses

Set controls (and connectors) as follows:

Control	Operation
PERIOD Switch	TRIG
TRIG/GATE INPUT Connector	Apply TTL rectangular pulse
INT 50Ω Switch	ON
WIDTH Switch	Set to range desired (but not ⎍)
Other Controls	Set as desired.

3.3.4 Manually Triggered Pulsos

Set controls (and connectors) as follows:

Control	Operation
PERIOD Switch	MAN **TRIG**
INT 50Ω Switch	**ON**

Control	Operation
WIDTH Switch	Set to range desired (but not ⊓⊔)
MAN TRIG	Push to trigger
Other Controls	Set as desired

3.3.5 Gated Pulses

Set up as in paragraph **3.3.1,** except set the width of the TRIG GATE INPUT pulse to allow the desired number of output pulses.

3.3.6 Pulses With Width Controlled Externally

Set up as in paragraph 3.3.3, except set WIDTH switch to ⊓⊔.

3.3.7 Double Pulses

For double pulses in any mode, additionally set controls as follows:

Control	Operation
DBL PULSE	ON
DELAY	Set for desired time between start of first pulse and second pulse of pulse pairs. (Since the same one-shot forms both pulses, a minimum recovery time is necessary.)

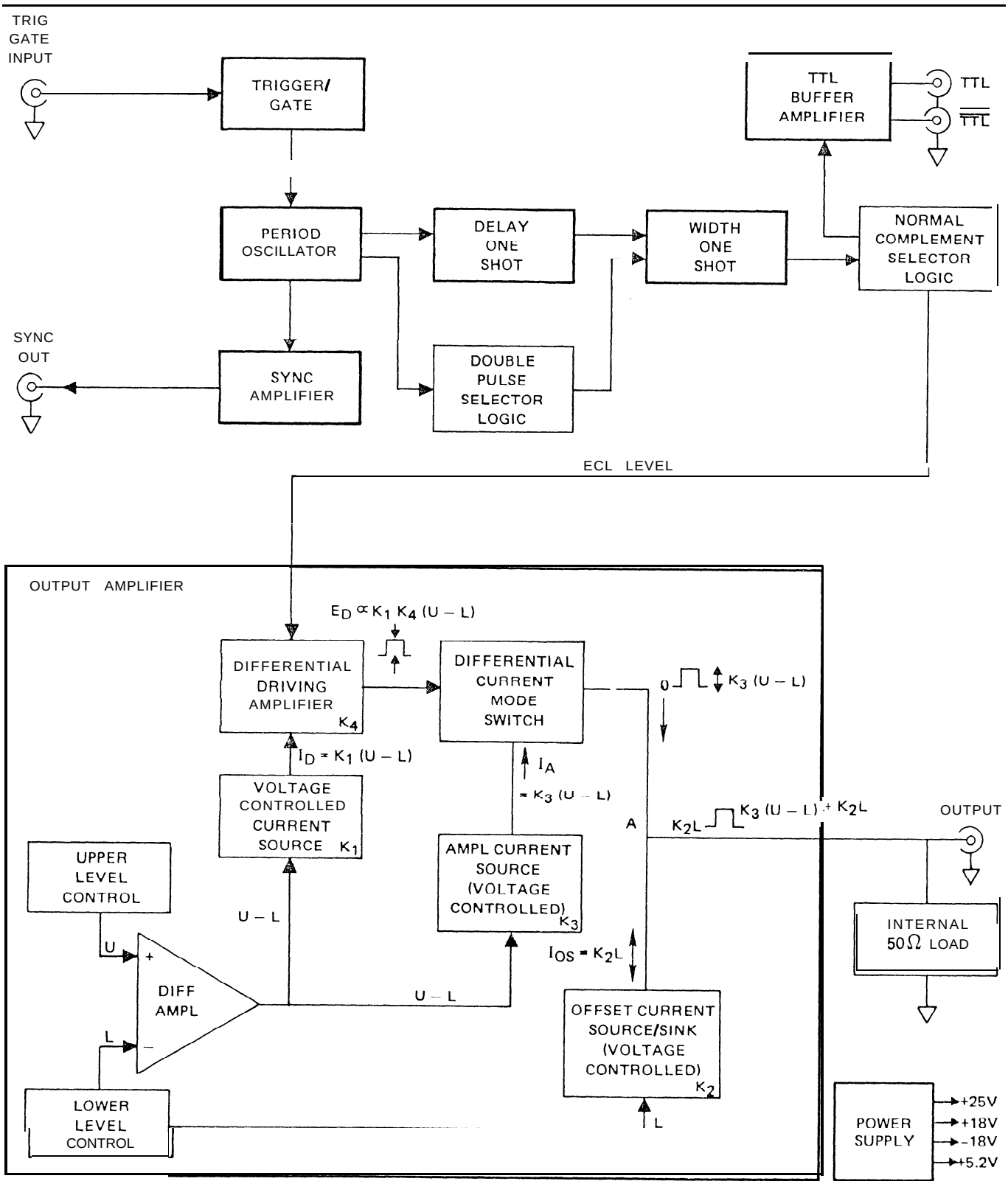


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 OVERALL BLOCK DIAGRAM

The Model 802 is made up of eight major circuit blocks: trigger/gate circuit, period oscillator, sync amplifier, delay one shot, width one shot, TTL buffer amplifier, output amplifier, and a power supply. (See figure 4-1.)

All the circuitry is on one PC board with a combination of ECL logic gates and discrete semiconductor devices. The ECL logic, in addition to making up individual circuit blocks, serves as a signal coupling medium between the blocks. The signal path changes depending on the mode selected.

4.2 PERIOD OSCILLATOR

A simplified diagram of the period oscillator, an ECL multivibrator, appears in figure 4-2.

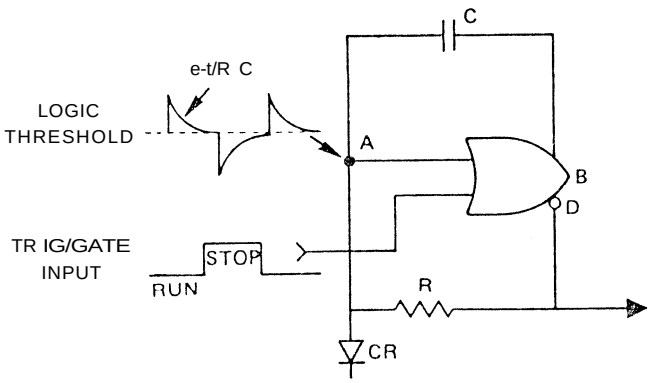


Figure 4-2. Simplified Diagram of the Period Oscillator

The RC time constant determines the charge and discharge rates for capacitor C and, therefore, the frequency of operation.

Positive feedback via the path through C results in a stable oscillator. Varying resistor R changes the frequency over a 10: 1 range. Note that since the charging and discharging current are equal but opposite, the resulting waveform has a **50%** duty cycle.

The oscillator may be gated via the trig/gate input. Whenever this input is high, it forces output D low and stops the oscillator. The oscillator starts synchronously when the input goes low.

4.3 TRIGGER/GATE CIRCUIT

The trigger circuit consists of an ECL gate connected to provide positive feedback which forms a Schmitt trigger. An input divider adjusts the trigger level to approximately +1.4V. This makes the input compatible with TTL logic. Triggering always occurs on the positive edge and the source can be either external or internal via the manual trigger switch.

The output of the trigger circuit is always connected to the oscillator. Gating occurs automatically. Whenever the input to the trigger circuit is 1.4V, it forces the trig/gate input of the oscillator high (figure 4-2) and stops the oscillator.

When the trigger mode is selected, node A of the oscillator is pulled low via diode CR. The IC now acts as an inverter to the trig/gate input and passes the signal on to the delay one shot.

4.4 SYNC CIRCUIT

The sync circuit acts as a buffer amplifier between the oscillator and the external equipment. It provides a TTL output level from a 50Ω source. The output from the sync circuit is an approximate square wave at the oscillator frequency.

When gating the generator, the sync signal should be taken from the gating source rather than the 802.

4.5 DELAY CIRCUIT

The delay one shot allows an adjustable time between the sync output and the leading edge of the final output pulse. The delay circuit consists of an ECL gate and discrete circuit one shot multivibrator. When the delay circuit is triggered by the oscillator, a timing capacitor is discharged by a constant current source until a threshold point is reached. The circuit then resets by rapidly recharging the timing capacitor. The output pulse from the ECL gate has a width proportional to the timing capacitor value and the magnitude of the current source. The pulse width is independent of the triggering rate as long as it is less than 70% of the trigger period.

4.6 WIDTH CIRCUIT

The width one shot determines the width of the output **pulse.** The width circuit, triggered by the trailing edge of the delay one shot, is identical in operation to the delay **circuit. In the double pulse** mode it is triggered on the leading and trailing edges of the delay one shot pulse. When the mode is selected, the delay and width one shots are disabled and the oscillator square wave passes through them to the output amplifier. An exclusive OR gate allows either phase of the width one shot output to be selected as the signal to drive the output amplifier.

4.7 TTL BUFFER AMPLIFIER

The output of the width one shot drives a current mode switch, the TTL buffer amplifier, in addition to the output amplifier. This switch is designed to drive TTL level signals into 50Ω loads. Both signal phases, TTL and $\overline{\text{TTL}}$, are available simultaneously.

4.8 OUTPUT AMPLIFIER

The output amplifier (figure 4-1) establishes the pulse lower level by passing a constant current through the 50Ω load. The current is provided by a voltage controlled current source programmed by the lower level control potentiometer. A current pulse of the proper amplitude is now added **at node** A **to this base line** for the duration of the width one shot time. The amplitude of the current pulse is equal to the difference between the upper and lower level controls (U − L). The upper level will be (U − L) + L = U at the output.

In order to generate a current pulse, the width one shot drives a current mode switch via a driving amplifier. The current mode switch connects a current source to the load whenever the output of the width one shot is high. The current source is voltage controlled and its output is equal to the difference between the upper and lower level controls (U − L).

The output of the driving amplifier varies in amplitude directly with the output level programmed by the level controls. This prevents overdriving the current mode switch and distorting the output at low levels.

Note that changing the lower level control will change both the base line and the current pulse amplitude which will cause the upper level to remain fixed. That is (U − L) + L = U, regardless of the value of L.

The internal 50Ω load may be switched in or out depending on the application.

4.9 POWER SUPPLY

The power supply converts the line voltage to four regulated dc voltages which power all the other circuit blocks.

4.10 MODES OF OPERATION

The major circuit block connections depend on the mode of operation selected. Block diagrams of the major modes and key waveforms are shown in figures 4-3 through 4-8.

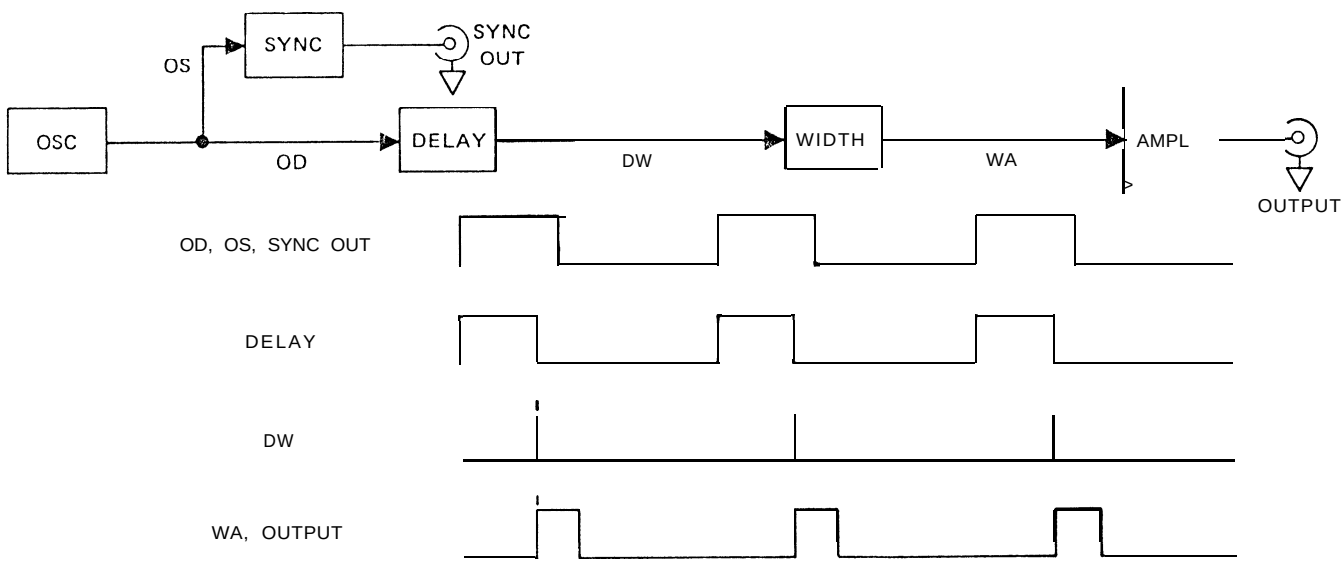


Figure 4-3. Continuous Mode

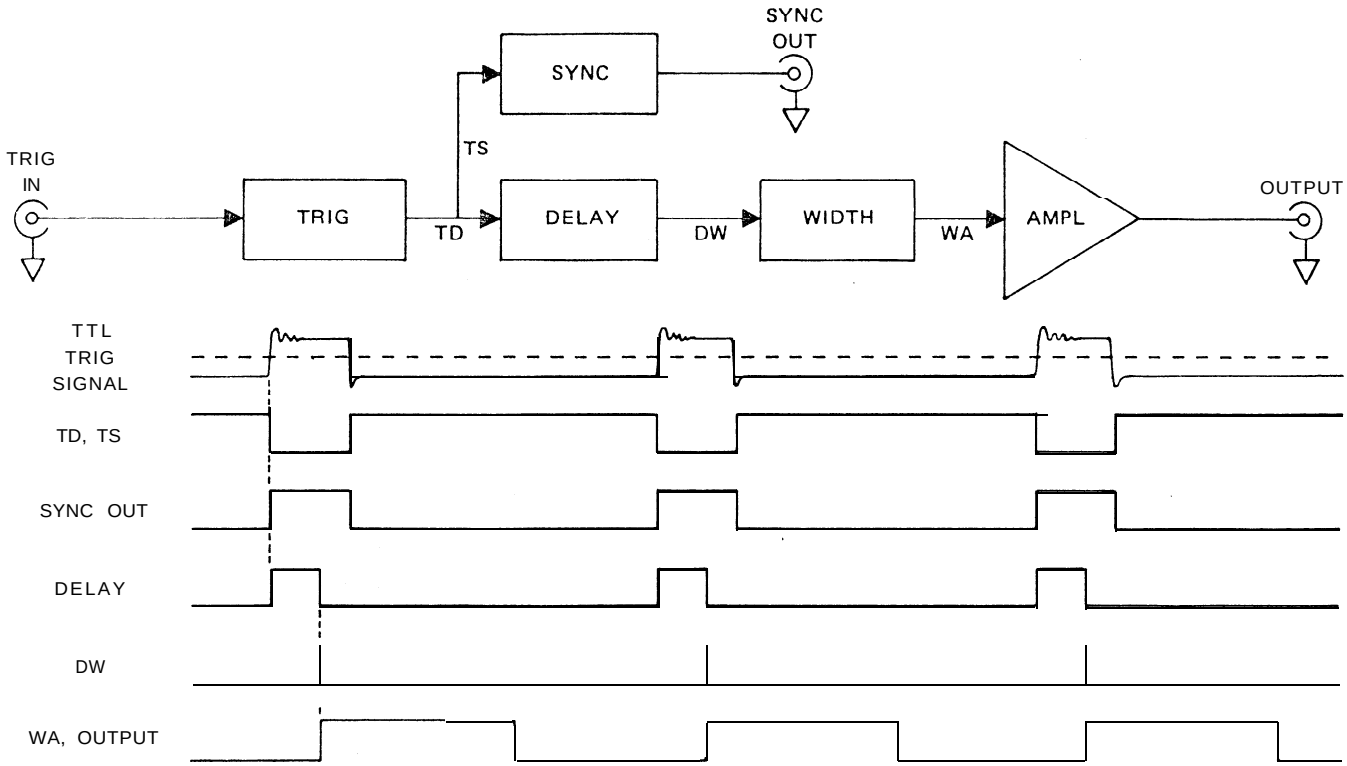


Figure 4-4. Trigger Mode

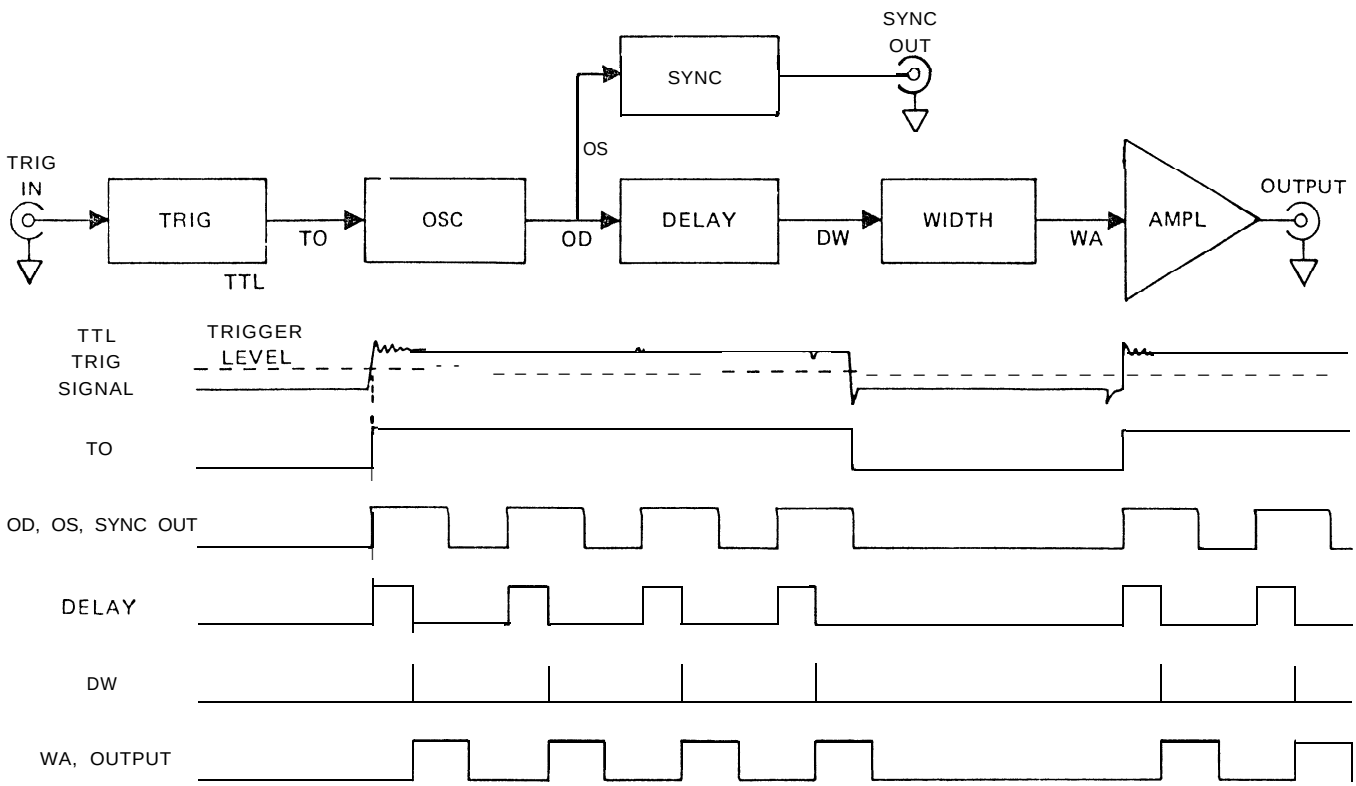


Figure 4-5. Gate Mode

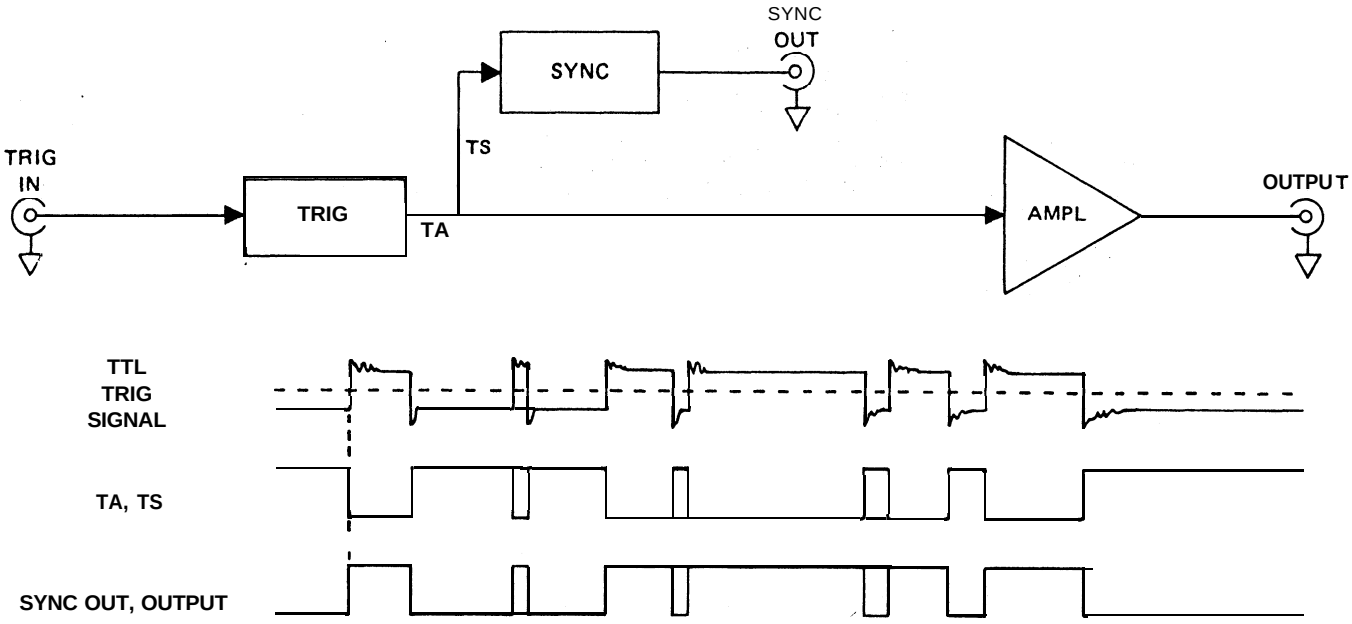


Figure 4-6. External Width Mode

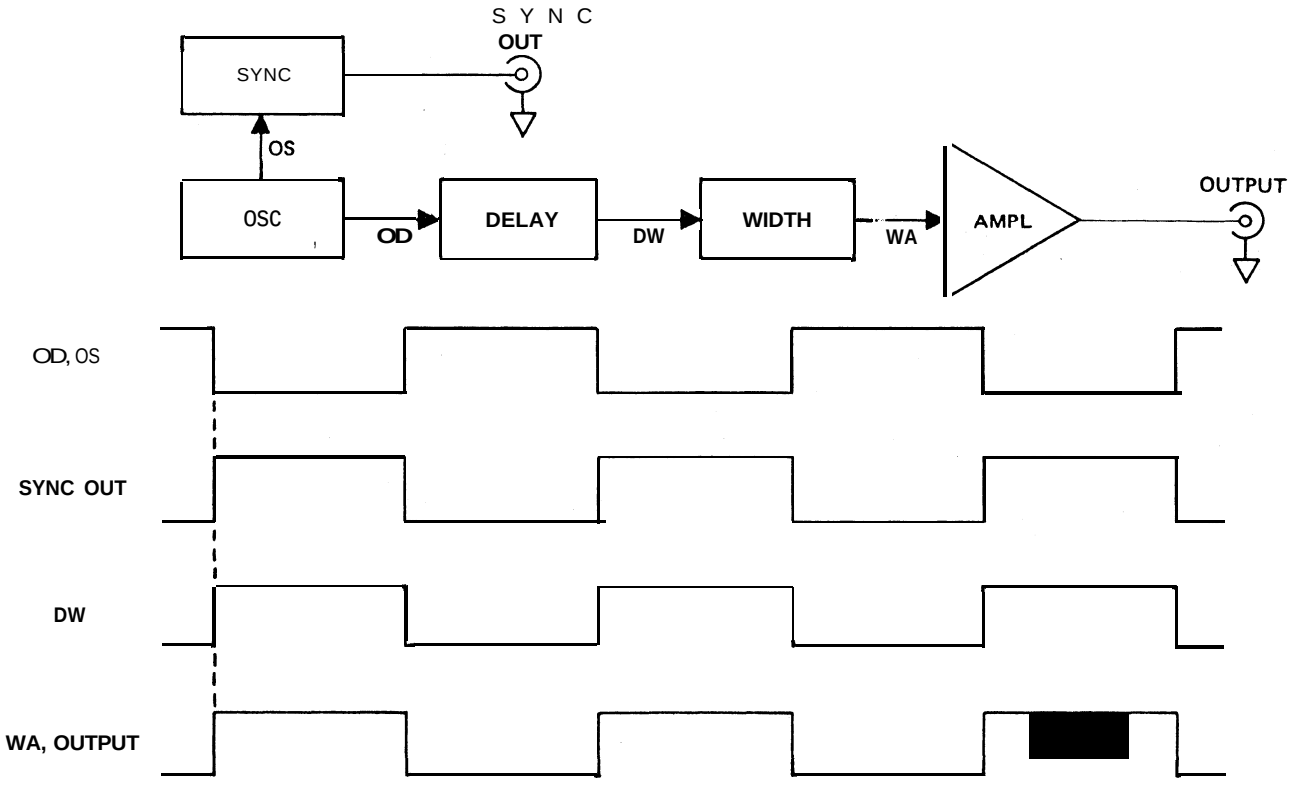


Figure 4-7. Continuous Square Wave Mode

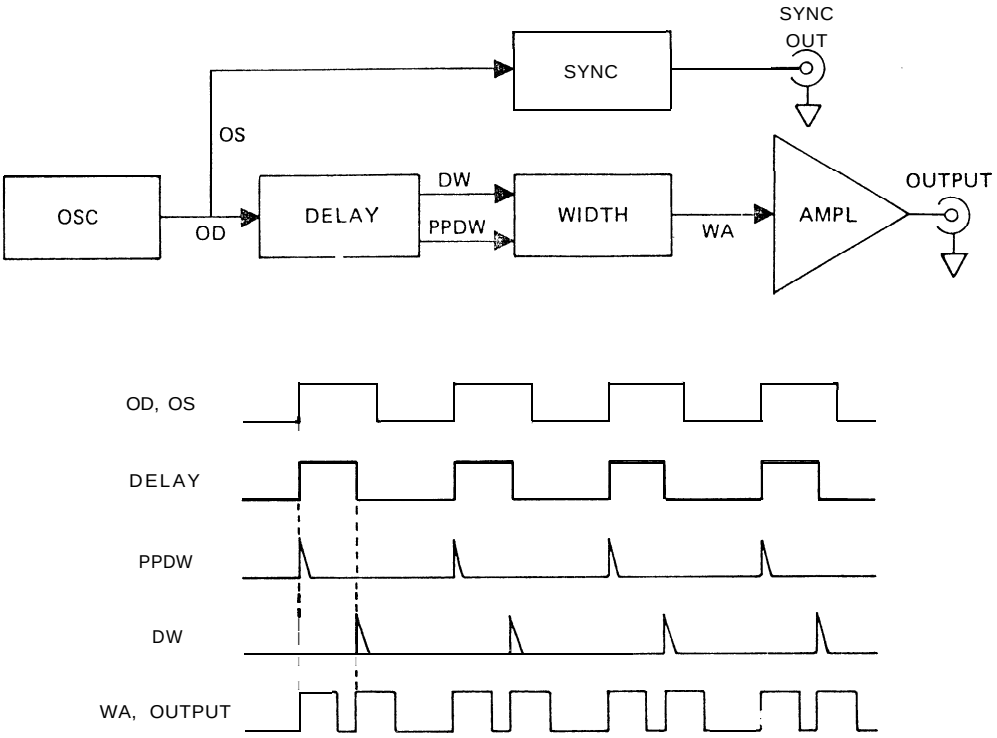


Figure 4-8. Continuous Double Pulse Mode