Agilent M8190A Arbitrary Waveform Generator

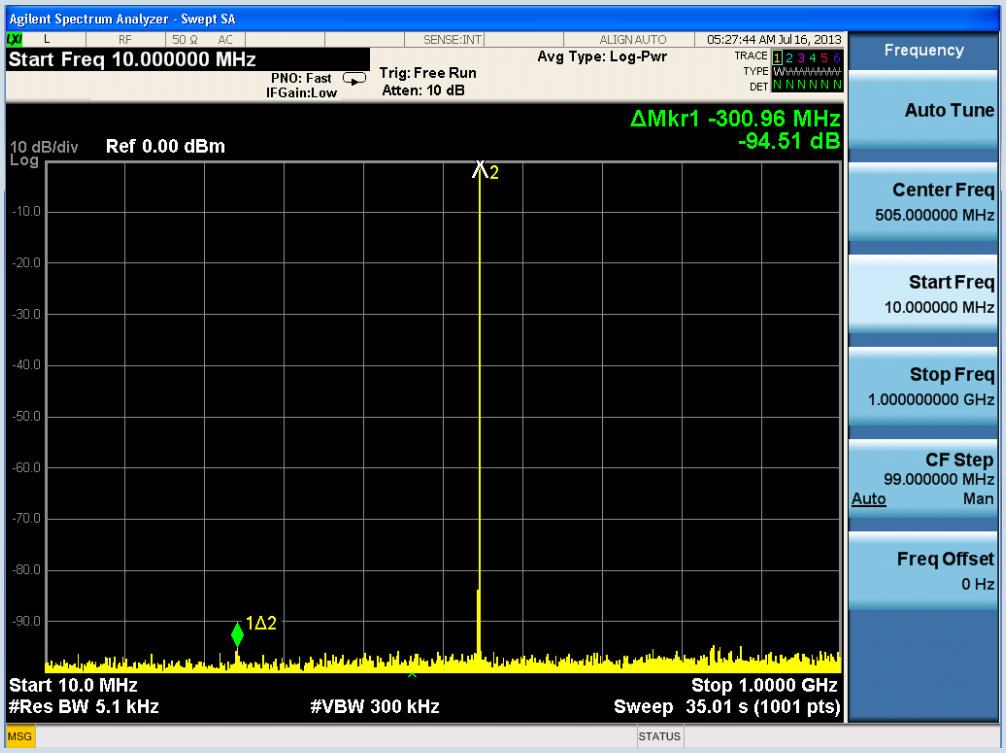
12 GSa/s Arbitrary Waveform Generator

Data Sheet
Version 1.4

Enhance your reality

Anticipate ___Accelerate ___Achieve

Agilent Technologies



HIGH RESOLUTION + WIDE BANDWIDTH IN AN AWG

M8190A at a glance

- Precision AWG with two DAC settings
  - 14-bit resolution up to 8 GSa/s
  - 12-bit resolution up to 12 GSa/s
- Variable sample rate from 125 MSa/s to 8/12 GSa/s
- Spurious-free-dynamic range (SFDR) up to 80 dBc typical
- Harmonic distortion (HD) up to –72 dBc typical
- Up to 2 GSa arbitrary waveform memory per channel with advanced sequencing
- Analog bandwidth 5 GHz
- Optional real-time digital signal processing in Agilent proprietary ASIC for:
  - Digital up-conversion to IF
  - Changing waveform parameters on the fly

Three amplifiers for different applications

- **Direct DAC**—optimized for best SFDR & HD
  - SFDR up to –80 dBc (typ), f_{out} = 100 MHz, measured DC to 1 GHz
  - Amplitude ~350 mVpp ... 700 mVpp, offset –20 mV ... +20 mV
  - Differential output
- **DC amplifier** [1]—optimized for serial data/time domain applications
  - Amplitude 500 mV_{pp} ... 1.0 V_{pp}; (overprogramming down to 150 mV possible) output voltage window: –1.0 V ... +3.3 V
  - $t_{rise/fall,\ 20\% - 80\%}$ < 60 ps
  - Differential output
  - **AC amplifier** [1]—optimized to generate high voltage, high bandwidth signals
  - 50 MHz to 5 GHz bandwidth
  - Single ended, AC coupled output
  - Amplitude: 200 mV_{pp} ... 2.0 V_{pp}
- Form-factor: 2 U AXIe module, controlled via external PC or AXIe system controller
- Supported software: Agilent Benchlink Waveform Editor, MATLAB, LABVIEW, Agilent Signal Studio Pulsebuilder, Signal Studio WLAN, Test automation software support for MHL and HDMI; planned support for Signal Studio Multitone

1. *AMP option*

ENHANCE YOUR REALITY

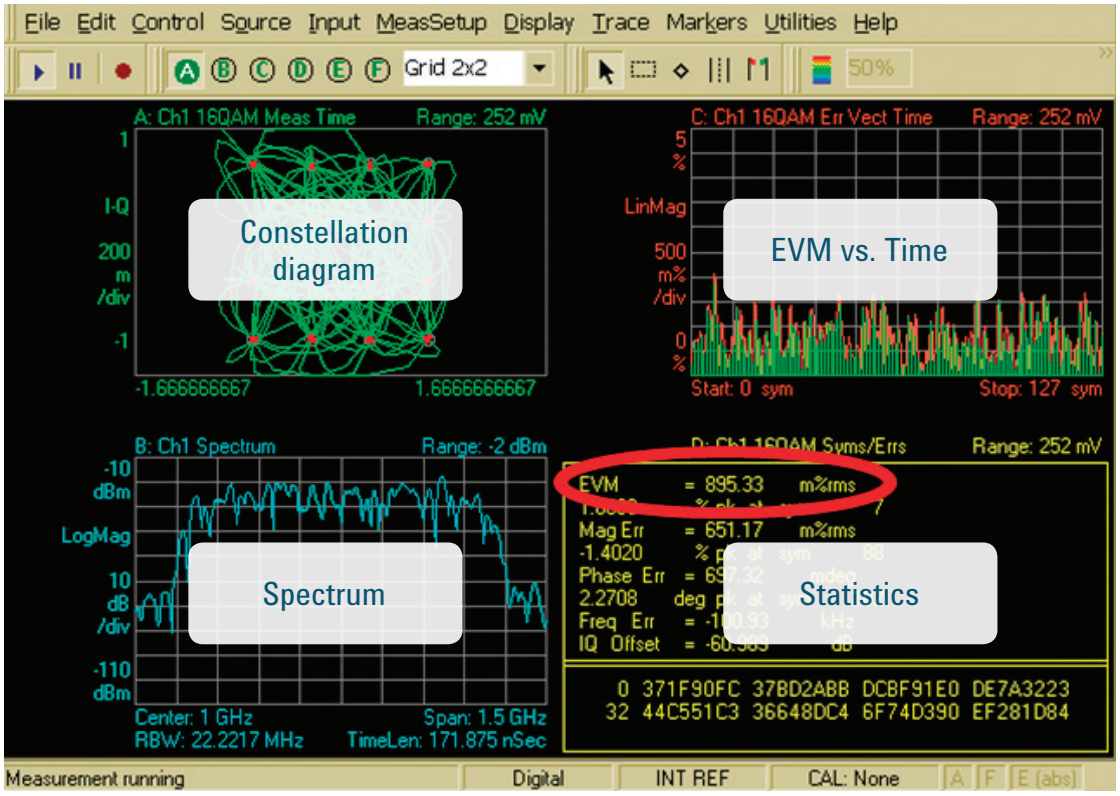
A better name for an advanced arbitrary waveform generator is a “signal scenario generator” or SSG.

This description signifies a level of versatility that enables you to set up complex real-world signals—whether you need precise signals to characterize the performance of a design or need to stress a device to its limits. From low-observable radar to high-density communications, testing is more realistic with precision arbitrary waveform generation from an SSG.

Take reality to the extreme: An Agilent AWG is the source of greater fidelity, delivering high resolution and wide bandwidth—simultaneously. This unique combination lets you create signal scenarios that push your designs to the limit and bring new insights to your analysis. Get bits and bandwidth—and enhance your reality.

High-quality signal generation is the foundation of reliable and repeatable measurements. The Agilent M8190A ensures accuracy and repeatability with 14-bit resolution, up to 8 GSa/s sampling rate and up to 80 dBc SFDR. High dynamic range and excellent vertical resolution gives you confidence that you are testing your device, not the signal source.

As an example, a test setup that exhibits a high error vector magnitude (EVM) reading might prevent you from seeing problems within your device under test (DUT). The level of reality possible with the M8190A minimizes problems like this.



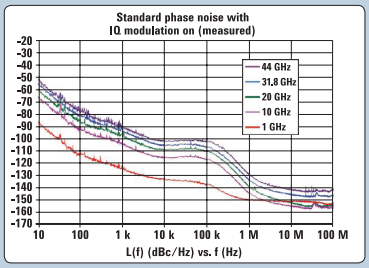
Get reliable, repeatable measurements from precise signal simulations

Optimize the output to match your application

An AWG is the most versatile signal scenario generator possible. Capabilities such as easy switching between 14-bit output at 8 GSa/s and 12-bit output at 12 GSa/s help you handle multiple applications and measurement requirements.

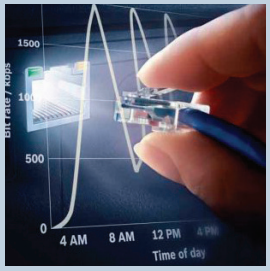
Because every application calls for different signal characteristics, the Agilent M8190A also contains three amplifiers that are optimized for I/Q signals, IF/RF output, or clean time-domain signals. You can switch between them as needed through software commands.

Optimized for different signal characteristics



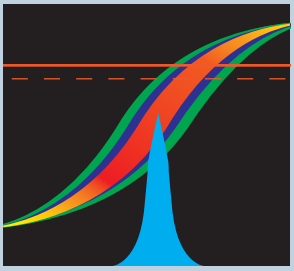
Best SFDR and HD

- Single-ended or differential output
- Amplitude 350 mV_{pp} ... 700 mV_{pp}, single-ended
- Offset –20 mV ... +20 mV
- Direct output
- Adjustable differential offset



High bandwidth high voltage

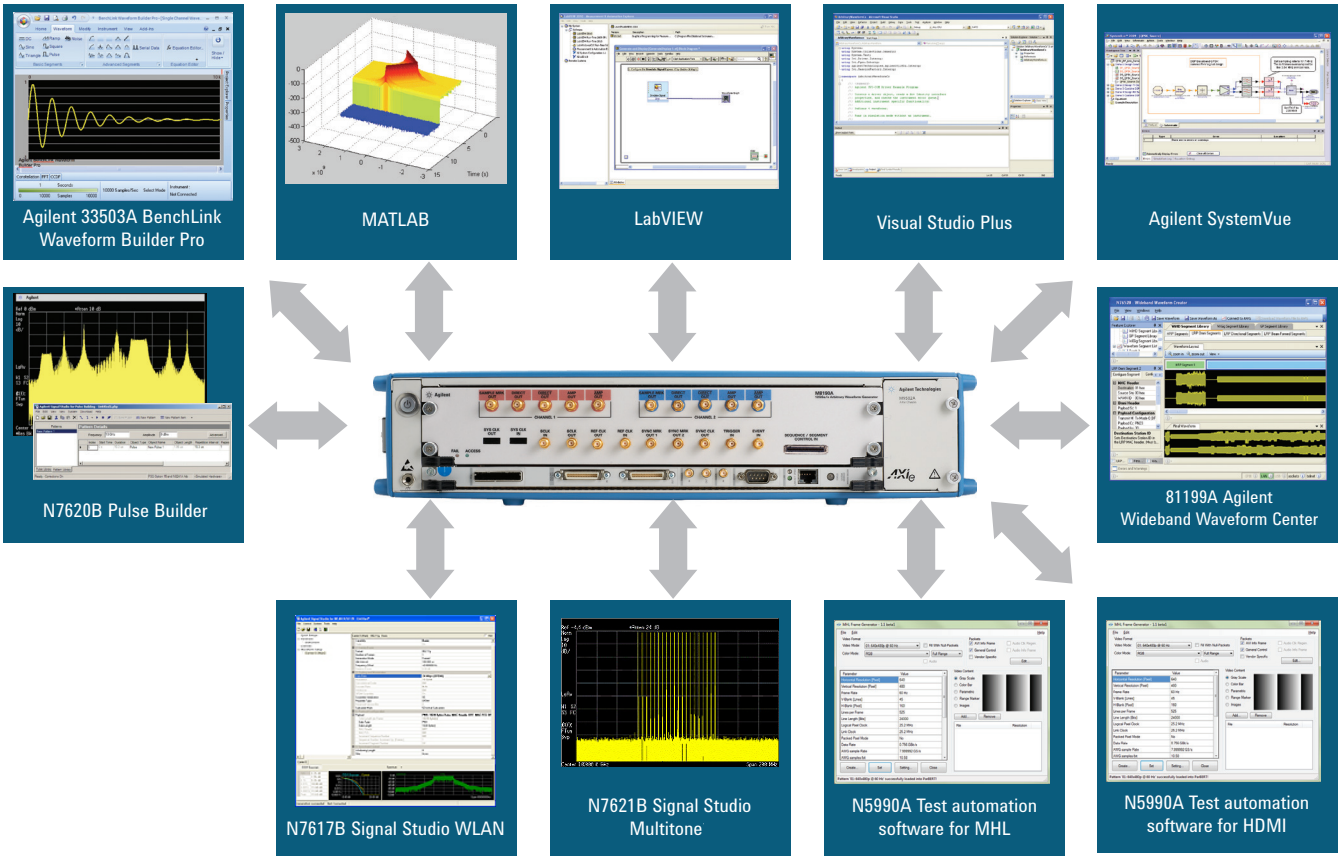
- Up to 5 GHz
- Single-ended, AC coupled output
- Amplitude 200 mV_{pp} to 2.0 V_{pp}, single-ended
- AC amplifier [1]



Time domain measurements low jitter

- Single-ended or differential, DC-coupled output
- Amplitude 500 mV_{pp} ... 1.0 V_{pp} single-ended
- Output voltage window –1.0 V to +3.3 V
- Transition times (20/80) < 60 ps
- DC amplifier [1]

1. AMP option



Create complex signal scenarios—efficiently

MEMORY

Highly realistic testing often requires long play times and long signal scenarios

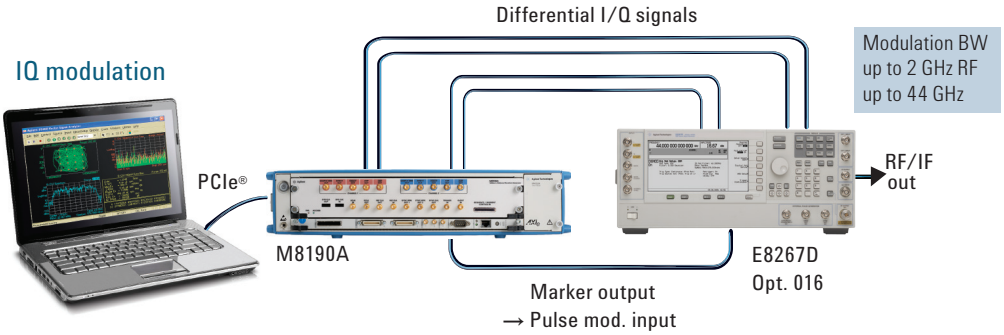
For example, 2 GSa of memory combined with advanced sequencing capabilities allow you to use the memory efficiently and effectively.

Direct access to individual memory segments is possible in real time through the dynamic sequence control input. You can create waveforms and download them into the M8190A using software applications such as Signal Studio Pulse Builder, Multi-tone and WLAN; SystemVue, MATLAB, LabView or your own routines written in C++, C# or Visual Basic.

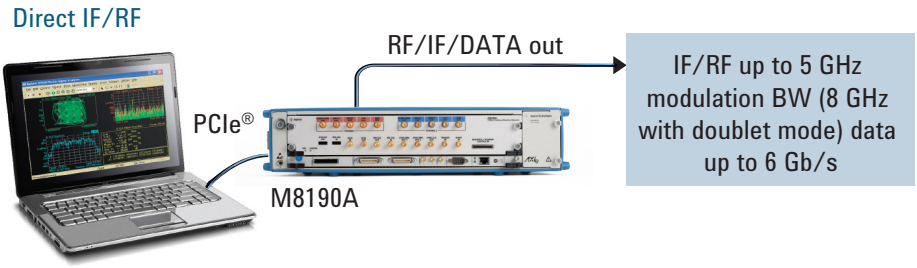
For sensitive applications, memory storage is not persistent: Memory contents are volatile and are erased when power is turned off.

Assemble the best configuration for your application

The typical test setup shown to the right covers high RF applications up to 40 or 60 GHz. In this case the M8190A generates differential I/Q signals that are sent to an upconverter such as the Agilent PSG signal generator. The M8190A is packaged in the AXIe form factor, which reduces system size, weight and footprint.



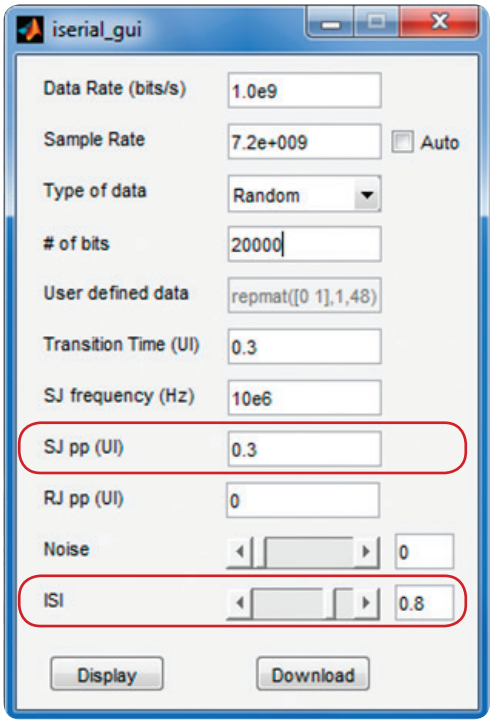
The block diagrams shown to the right illustrate configurations for I/Q modulation and direct IF/RF output. The M8190A supports direct generation of IF signals: Because this is done digitally, signal quality is outstanding. The instrument provides an analog bandwidth of 5 GHz; if higher output frequency is needed a mixer must be added to the configuration.

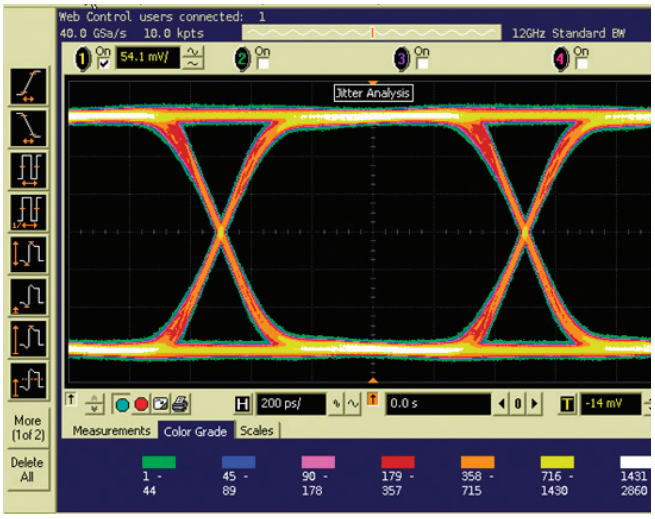


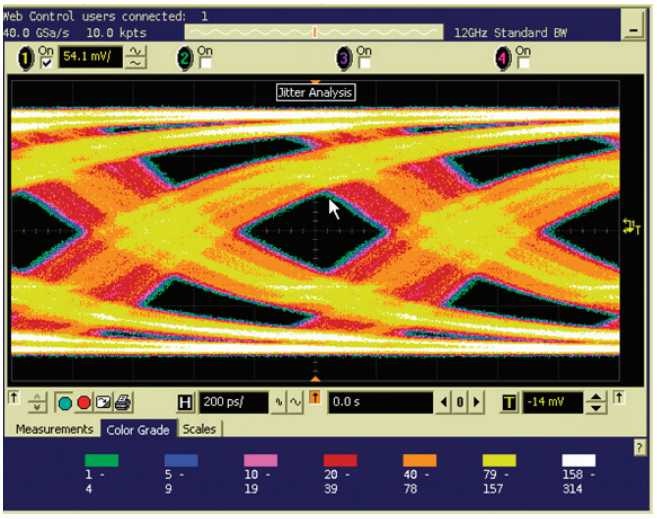
MULTI-LEVEL SIGNALS

Jitter and noise cause misalignment of edges and levels, resulting in data errors.

The M8190A is equipped to ensure flexible modifications to fit new distortion requirements by simply adapting the waveform itself. You can easily mimic analog imperfections that occur in real-world environments by using mathematical description in tools such as MATLAB. This minimizes the need for additional hardware while preserving the ability to create realistic signal simulations.







Generate multi-level signals with programmable ISI and jitter up to 6 Gb/s

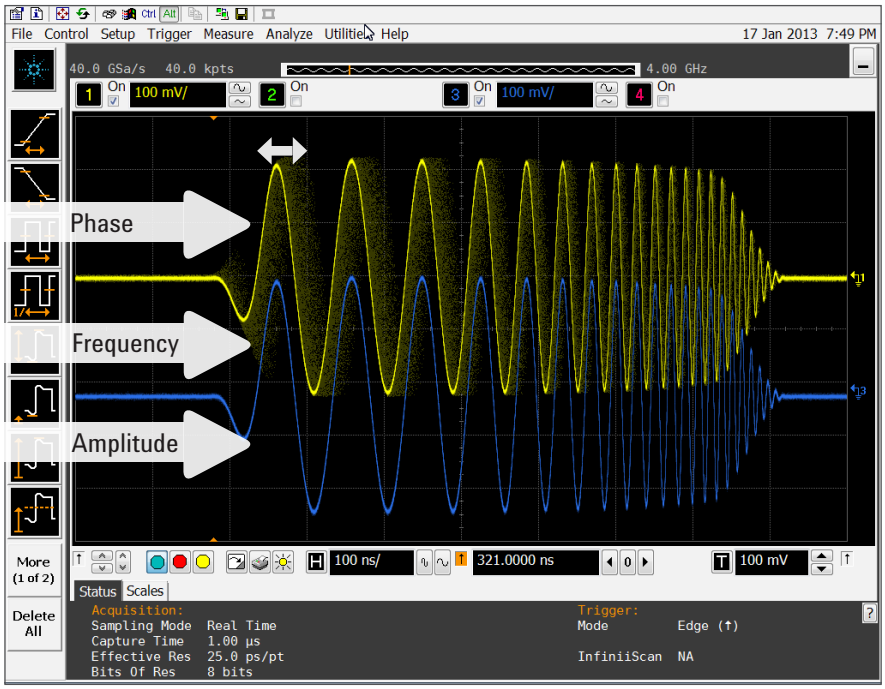
In aerospace and defense, technology is evolving to wider bandwidths without compromising on resolution.

The foundation is digital technology, which is becoming more prevalent because it provides advantages such as reduced size, lower power requirements, better calibration and faster volume scans.

When developing radar systems, real-life testing is very expensive. Simulations with highly realistic signals help reduce the cost of system testing. The Agilent M8190A addresses these needs with three key capabilities: wide bandwidth, high resolution and long play times.

Real-time digital signal processing with Agilent proprietary ASIC

Digital up-conversion takes testing one step further. The wide bandwidth allows generating the IF signal directly. The IQ data will be upconverted digitally in hardware which gives you best signal quality in the desired frequency range. The frequency resolution is very precise with sample clock down to the picosecond range. In addition efficient memory usage allows to extend the playtime by up to 1 million times. For example for a radar signal the waveform needs to be stored only once and amplitude, frequency and phase are stored independently. Precise carrier frequency, phase and amplitude settings is possible in real-time under sequencer control. Even complex operations such as frequency sweep are possible.



Radar chirp with phase changes on the fly

Push radar and electronic warfare designs farther with highly realistic signal scenarios

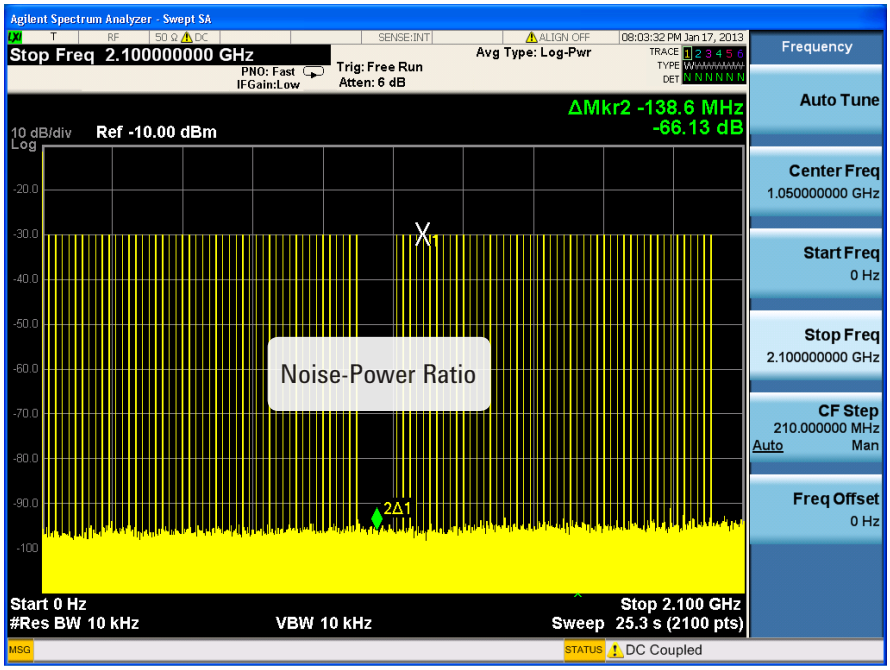
HEADROOM

Accurate emulation of transmissions—from ground station to airborne transceiver to distant ground station—includes interference, fading and more.

High numbered digital modulations transport more data in the same bandwidth, but tend to produce inaccurate levels and phase angles. Detailed testing becomes very important.

As a result, it is necessary to create high-quality signals with 14-bit resolution SFDR less than –80 dBc. This excellent SFDR ensures that tones stand out from distortion, even with hundreds of tones. The 2 GSa memory ensures that you can store more than one signal scenario and simply switch between segments via direct memory access and the dynamic sequence control input.

The M8190A gives you the versatility to define new signals—proprietary, next-generation and beyond. The 5 GHz modulation bandwidth gives you enough headroom to test and address next-generation modulation schemes.



Multi-tone signal — 100 tone from 0 to 2.1 GHz
(Fs = 7.2 GHz, sin(x)/x compensated)

Build a strong foundation for highly reliable satellite communications

PRODUCT STRUCTURE

The AWG has a modular product structure and requires an AXIe chassis (please see page 13)

M8190A	Option	Software upgradeable	Comment
1 channel	001		MUST order either 001 or 002
2 channel	002		
14 bit /8 GSa/s	14B	X	MUST order either 14B or 12G or both options
12 GSa/s/12 bit	12G	X	
Additional DC and AC amplifier	AMP	X	
Digital up-conversion to carrier frequency	DUC	X	
Upgrade from 128 MSa to 2 GSa memory per channel	02G	X	2 channel version requires Option 02G (quantity 2)
Sequencer	SEQ	X	
Fast switching	FSW	X	Fast switching for 12 GSa/s requires export control license FSW is included in 14B option
ISO 17025	1A7		Calibration options
Z540	Z54		

Upgrades from revision 1 to revision 2 is possible with the option UBE. Hardware upgrade is a division upgrade.

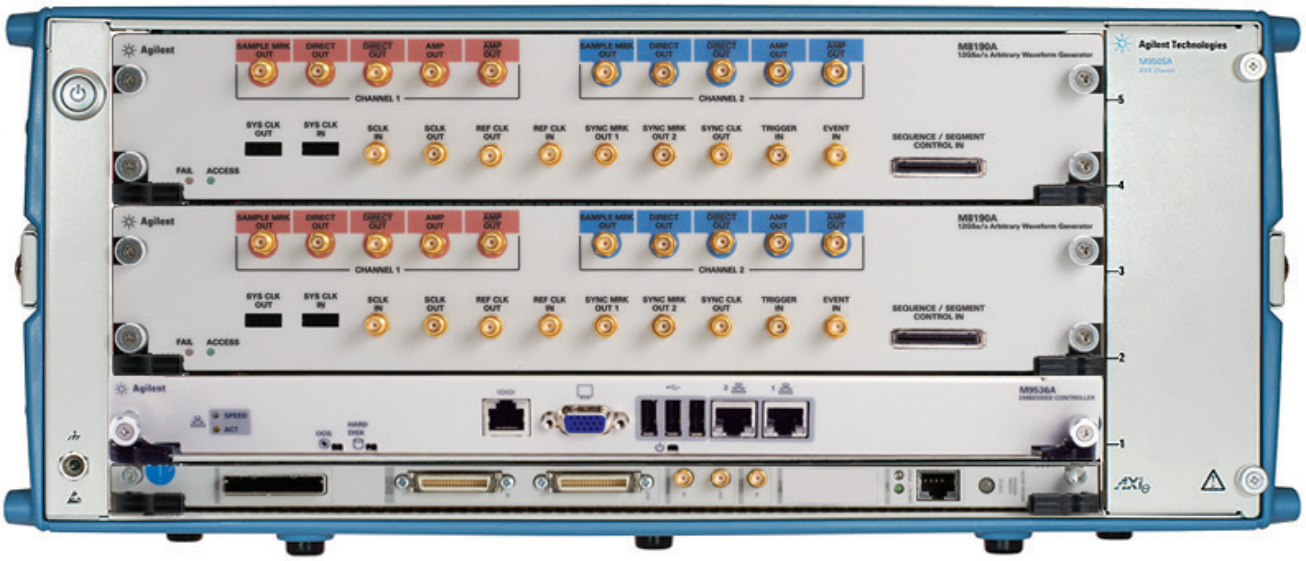
Bundles including AXIe chassis are available under:

M8190A -BU1 5 slot chassis, with embedded PC 16 GB RAM and Windows Embedded Standard 7 operating system: 64 bit
M8190A -BU2 2 slot chassis with PCIe cable and adapter. Choice between desktop and laptop cabling
M8190S Multichannel Arbitrary Waveform Generator System (4- & 8 channels are selectable)

Acccessories

M8190A-801	Microwave phase matched balun, 6.5 GHz, max SMA jack
M8190A-805	Low pass filter, 2800 MHz, max SMA, VLF 2850+
M8190A-806	Low pass filter, 3900 MHZ max SMA, VLF 3800+
M8190A-810	Cable assembly coaxial–50 Ω, SMA to SMA, 457 mm length
M8190A-811	Cable assembly coaxial–50 Ω, SMA to SMA, 1220 mm length
M8190A-815	Dynamic control input cable
M8190A-820	Connector-RF, SMA termination, plug straight, 50 Ω, 12.4 GHz, 0.5 W

Two slot AXIe chassis with M8190A AWG



Five slot AXIe chassis with two M8190A AWG; can contain an embedded controller

AXIe

The M8190A is a modular instrument packaged in the AXIe form factor. AXIe is a new open standard for high-performance, modular instrumentation, and incorporates the best features of other modular formats including VXIbus, LXI and PXI. Agilent offers a line of scalable chassis in this powerful format. Along with controller options, these AXIe chassis can form the basis of high-performance, AXIe-based test systems.

Two form factors are available: two-slot and five-slot chassis. These include an embedded AXIe system module that does not occupy a module slot. In addition, an AXIe controller is an entire system that can control the AWG. This controller consumes one module slot in the chassis.

The chassis can be used on the bench or in a rack, occupying only 4U of rack space. Agilent computer I/O cards are also available for AXIe systems.

- M9502A: Two-slot AXIe chassis with ESM
- M9505A: Five-slot AXIe chassis with ESM
- M9045B: PCIe laptop card adapter Gen 1 x4
- M9048A: PCIe desktop card adapter Gen 2 x8
- Y1200B: x4 – x8 PCIe cable
- Y1202A: x8 – x8 PCIe cable
- M9536A: Embedded AXIe controller
- M8192A Multi-Channel Synchronization Module for M8190A AWG

PERFORMANCE SPECIFICATION

General characteristics

Characteristics	Description	
Digital to analog converter		
Option: –14B	Resolution Sample rate	14 bit 125 MSa/s to 8 GSa/s
Option: –12G	Resolution Sample rate	12 bit 125 MSa/s to 12 GSa/s
Sin (x)/x roll-off (mathematically calculated)		
Option: –14B	Sin (x)/x (–1 dB) Sin (x)/x (–3 dB)	2.1 GHz @ 8 GSa/s 3.5 GHz @ 8 GSa/s
Option: –12G	Sin (x)/x (–1 dB) Sin (x)/x (–3 dB)	3.1 GHz @ 12 GSa/s 5.3 GHz @ 12 GSa/s

Frequency switching characteristics

Effective output frequency (f_{max} is determined as $f_{Sa,max}/2.5$)		
Option: –14B	f_{max} = 3.2 GHz	
Option: –12G	f_{max} = 4.8 GHz	
Effective frequency switching time [1]		
Option: –14B [2]	313 ps (= 1/ f_{max})	
Option: –12G	No option:	–FSW 105 µs to 210 µs
Option: –12G	Option:	–FSW 208 ps (= 1/f_{max})

1. *Determines the minimum time needed to switch between selected segments in sequence mode.*
2. *Option FSW does not affect switching time in 14 bit mode (Option 14B).*

Direct out1/direct out2

Characteristics	Description
Type of output	Single-ended [1] or differential, DC-coupled
Skew between normal and complement outputs	0 ps (nom)
Skew accuracy between normal and complement outputs	± 5 ps (typ)
Impedance	50 Ω (nom)
Amplitude control	Specified into 50 Ω
Range, single-ended (DNRZ/NRZ Mode) [6]	350 mV_{p-p} to 700 mV_{p-p}
Resolution	30 µV (nom)
DC accuracy, offset = 0 V (DNRZ/NRZ Mode) [6]	± (1.5% + 15 mV) (spec)
Offset	–20 mV to + 20 mV, single-ended into 50 Ω
Offset resolution	60 µV (nom)
DC offset accuracy	± 10 mV (spec) Common mode offset and differential offset is seperately adjustable
Connector type	SMA

1. Unused output must be terminated with 50 Ω to GND.
6. Doublet mode does not allow DC signal generation.

NRZ/DNRZ mode

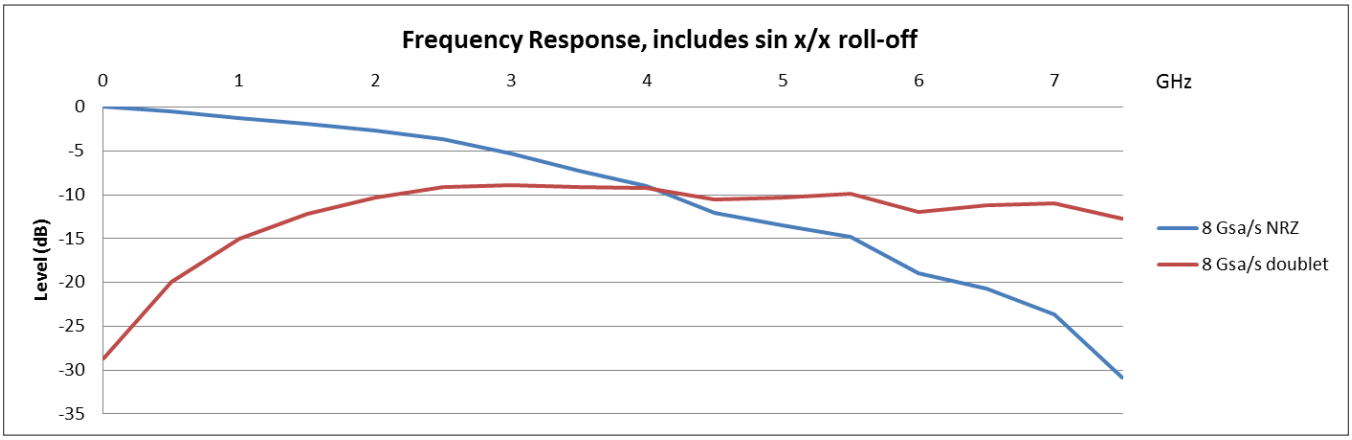
Bandwidth (3 dB) [2]	3.0 GHz (typ)
Bandwidth (5 dB)	5.0 GHz (typ)
Harmonic distortion 7.2 GSa/s [3, 5]	–72 dBc (typ, f_{out} = 100 MHz) –68 dBc (typ), f_{out} = 10 MHz ... 500 MHz, measured DC to 3 GHz –60 dBc (typ) , f_{out} = 500 MHz ... 3000 MHz, measured DC to 3 GHz
Harmonic distortion 12 GSa/s [4, 5]	–54 dBc (typ) f_{out} = 100 MHz –50 dBc (typ) f_{out} = 10 MHz ... 5000 MHz, measured DC to 5 GHz
SFDR in 14 bit mode [3, 5] (excluding harmonic distortion)	In Band Performance: -90 dBc (typ), fout = 100 MHz, measured DC to 2 GHz -80 dBc (typ), fout = 10 MHz...500 MHz, measured DC to 500 MHz -76 dBc (typ), fout = 500 MHz...1 GHz, measured DC to 1 GHz -68 dBc (typ), fout = 1 GHz...2 GHz, measured DC to 2 GHz -62 dBc (typ), fout = 2 GHz...3 GHz, measured DC to 3 GHz Adjacent Band Performance: -80 dBc (typ), fout = 10 MHz...500 MHz, measured DC to 1.5 GHz -73 dBc (typ), fout = 500 MHz...1 GHz, measured DC to 3 GHz -68 dBc (typ), fout = 1 GHz...2 GHz, measured DC to 3 GHz -62 dBc (typ), fout = 2 GHz...3 GHz, measured DC to 3 GHz
SFDR in 12 bit mode [4, 5] (excluding harmonic distortion)	In Band Performance: -90 dBc (typ), fout = 100 MHz, measured DC to 2 GHz -80 dBc (typ), fout = 10 MHz...500 MHz, measured DC to 500 MHz -78 dBc (typ), fout = 500 MHz...1 GHz, measured DC to 1 GHz -73 dBc (typ), fout = 1 GHz...2 GHz, measured DC to 2 GHz -68 dBc (typ), fout = 2 GHz...3 GHz, measured DC to 3 GHz -60 dBc (typ), fout = 3 GHz...5 GHz, measured DC to 5 GHz Adjacent Band Performance: -80 dBc (typ), fout = 10 MHz...500 MHz, measured DC to 1.5 GHz -73 dBc (typ), fout = 500 MHz...1 GHz, measured DC to 3 GHz -68 dBc (typ), fout = 1 GHz...2 GHz, measured DC to 5 GHz -64 dBc (typ), fout = 2 GHz...3 GHz, measured DC to 5 GHz -60 dBc (typ), fout = 3 GHz...5 GHz, measured DC to 5 GHz
Two-tone IMD [3]	TTIMD = –73 dBc (typ), f_{out1} = 499.5 MHz, f_{out2} = 500.5 MHz

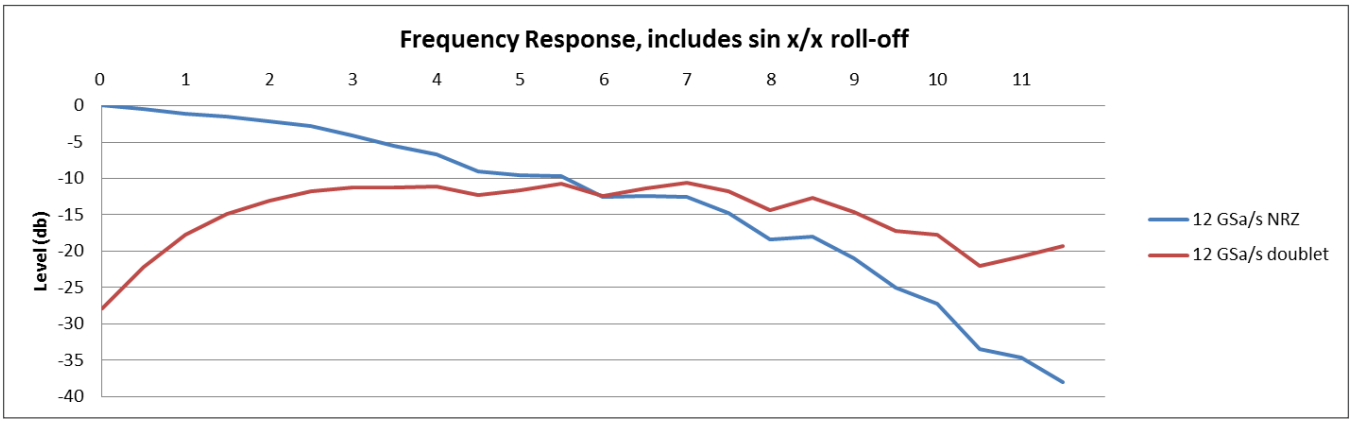
2. t_r bandwidth: BW = 0.25/t_r.
3. SCLK = 7.2 GSa/s, amplitude = 700 mV_{p-p}, double NRZ mode, excluding $f_{Sa} – 2 * f_{out}$, $fSa – 3 * f_{out}$.
4. SCLK = 12 GSa/s, amplitude = 700 mVp-p, double NRZ mode, excluding $f_{Sa} – 2 * f_{out}$, $fSa – 3* f_{out}$.
5. Measured with a balun such as the 5310A from Pico Second Pulse Labs plus 10 dB attenuator.
6. Doublet mode does not allow DC signal generation.

Doublet mode

Characteristics	Description
Bandwidth	See frequency plot (measured) 8 GHz/12 GHz, single ended
Harmonics 14 bit doublet mode [1] 8 GSa/s	f_{out} = 5400 MHz ... 6500 MHz measured 5.4 GHz to 6.5 GHz, no harmonics in this range
Harmonics 12 bit doublet mode [2] 12 GSa/s	f_{out} = 8100 MHz ... 9900 MHz, measured 8.1 GHz to 9.9 GHz, no harmonics in this range
SFDR in 14 bit doublet mode [1] 8 GSa/s (excluding harmonic distortion)	–48 dBc (typ) f_{out} = 5400 MHz ... 6500 MHz, measured 5.4 GHz to 6.5 GHz, Single ended
SFDR in 12 bit doublet mode [2] 12 GSa/s (excluding harmonic distortion)	–44 dBc (typ) f_{out} = 8100 MHz ... 9900 MHz, measured 8.1 GHz to 9.9 GHz, Single ended

1. *SCLK = 8 GSa/s, amplitude = 700 mV_{p-p}, double NRZ mode, excluding $f_{Sa} - 2 * f_{out}$, $f_{Sa} - 3 * f_{out}$.*
2. *SCLK = 12 GSa/s, amplitude = 700 mV_{p-p}.*





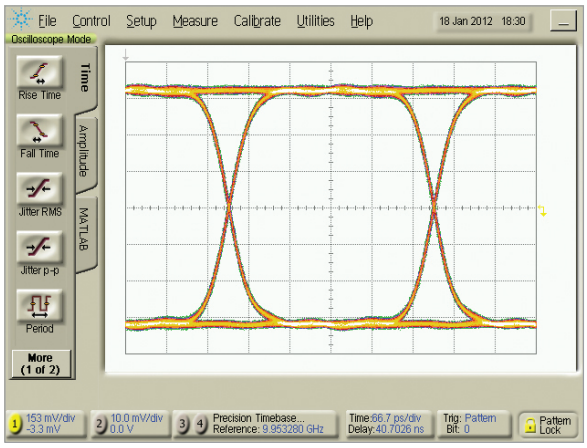
Two selectable output paths per channel are available when Option AMP is installed: 1) DC output path 2) AC output path.

Amp out1/amp out2

DC output

Characteristics	Description
Output type	Single-ended [1] or differential, DC-coupled
Impedance	50 Ω (nom)
Amplitude	500 mV_{pp} to 1.0 V_{pp}, single-ended into 50 Ω (overprogramming down to 150 mV possible)
Amplitude resolution	300 µV (nom)
DC amplitude accuracy	± (2.5% + 10 mV) (nom) [2]
Voltage window	–1.0 V to + 3.3 V [3], single-ended into 50 Ω
Offset resolution	600 µV (nom)
DC offset accuracy	± 2.5% ± 10 mV (typ) ± 4% of amplitude (typ) [4]
Termination voltage window	–1.5 V to + 3.5 V [3]
Termination voltage resolution	300 µV (nom)
Skew between normal and complement outputs	0 ps (nom)
Skew accuracy between normal and complement outputs	± 5 ps (typ)
Rise/fall time (20% to 80%)	< 60 ps (typ) [5]
Jitter (peak-peak)	15 ps (typ) [5]
Overshoot	5% (typ) [6]
Connector type	SMA

1. *Unused output must be terminated with 50 Ω to the termination voltage.*
2. *Termination voltage = 0 V; adjusted at 23 °C ambient temperature, amplitude reduces by 2 mV/°C (typ) for ambient temperature above 23 °C, amplitude increases by 5 mV/°C (typ) for ambient temperature below 23 °C[3].*
3. *Termination voltage window: offset ± 1V.*
4. *Termination voltage = 0 V.*
5. *PRBS $2^{11} - 1$, f_{Sa} = 12 GSa/s, data rate = 3 Gb/s, triggered on sample clock out, NRZ mode.*



Eye pattern with amplitude 1000 mV with 0 V offset

AC output

Characteristics	Description
Output type	Single-ended, AC coupled Front-panel marking: amp out1 for channel 1; amp out2 for channel 2
Impedance	50 Ω (nom)
Amplitude	200 mV_{pp} to 2.0 V_{pp} [1], single-ended into 50 Ω
Amplitude resolution	0.25 dB (nom)
Amplitude accuracy	± 0.5 dB [1] (typ)
Bandwidth (3 dB)	50 MHz to 5 GHz (typ)
Harmonic distortion [2]	< –39 dBc (typ), f_{out} = 375 MHz, measured DC to 3 GHz
	< –37 dBc (typ), f_{out} = 100 MHz ... 3000 MHz, measured 100 MHz to 3 GHz
Harmonic distortion [3]	< –39 dBc (typ) f_{out} = 375 MHz, measured DC to 5 GHz
	< –37 dBc (typ) f_{out} = 100 MHz ... 5000 MHz, measured DC to 5 GHz
SFDR in 14 bit mode [2] (excluding harmonic distortion) [5]	
	< –60 dBc (typ), f_{out} = 100 MHz ... 2000 MHz, measured 100 MHz to 3000 MHz
	< –56 dBc (typ), f_{out} = 2000 MHz ... 3000 MHz, measured 100 MHz to 3000 MHz
SFDR in 12 bit mode [3] (excluding harmonic distortion)	
	< –60 dBc (typ), f_{out} = 100 MHz ... 2000 MHz, measured 100 MHz to 5000 MHz
	< –56 dBc (typ), f_{out} = 2000 MHz ... 3000 MHz, measured 100 MHz to 5000 MHz
	< –50 dBc (typ), f_{out} = 3000 MHz ... 5000 MHz, measured 100 MHz to 5000 MHz
Amplitude flatness [4]	100 MHz to 1 GHz (typ), + 1.5 dB to –0.5 dB 100 MHz to 4 GHz (typ) +/- 0.1 dB with calibration / pre-distortion
	1 GHz to 4 GHz (typ), –2 dB to + 3 dB
Two-tone IMD [2]	TTIMD = –46 dBc (typ), f_{out1} = 999.5 MHz, f_{out2} = 1000.5 MHz
Connector type	SMA

1. *500 MHz sine wave.*
2. *SCLK = 7.2 GSa/s, amplitude = 1 V_{p-p}, 14 bit mode, double NRZ mode, excluding $f_{Sa} - 2*f_{out}$, $f_{Sa} - 3*f_{out}$.*
3. *SCLK = 12 GSa/s, amplitude = 1 V_{p-p}, 12 bit mode, double NRZ mode, excluding $f_{Sa} - 2*f_{out}$, $f_{Sa} - 3*f_{out}$.*
4. *SCLK = 12 GSa/s, amplitude = 1 V_{p-p}; normalized to 100 MHz; 12 bit mode, includes sin (x)/x compensation.*
5. *SFDR numbers for interpolation mode are the same as the SFDR numbers for 14 bit mode.*
   For further specification please see the digital up-conversion specification.

Marker outputs

Characteristics	Description
Number of markers	Two markers per channel: Sample marker Sync marker
Output type	Sample marker: single-ended Sync marker: single ended

Sync marker out1/sync marker out2

Output impedance	50 Ω (nom)
Timing resolution [1]	N sample clock cycles (N = 64 in 12 bit mode; N = 48 in 14 bit mode)
Level	
Voltage window	–0.5 V to 2.0 V
Amplitude	200 mV_{pp} to 2.0 V_{pp}
Resolution	10 mV
Accuracy	± (10% + 25 mV) (typ)
Rise/fall time (20% to 80%)	150 ps (nom)
Width [1]	User-defined in multiples of N sample clock cycles (N = 64 in 12 bit mode; N = 48 in 14 bit mode)
Connector type	SMA

Sample marker out1/sample marker out2

Timing resolution [1]	1 sample clock cycle
Level	
Voltage window	–0.5 V to 2.0 V
Amplitude	200 mV_{pp} to 2.0 V_{pp}
Resolution	10 mV
Accuracy	± (10% + 25 mV) (typ)
Rise/fall time (20% to 80%)	150 ps (nom)
Width	49 sample clocks in 12 bit mode 40 sample clocks in 14 bit mode
Random jitter	5 ps RMS (typ)
Connector type	SMA

1. See characteristics digital up-conversion if interpolation is enabled.

A common trigger/gate input for both channels is provided on the front panel. This input is used to start a sequence or a scenario.

Trigger/gate and event input

Characteristics	Description
Input range	–5 V to +5 V
Threshold	
Range	–5 V to +5 V
Resolution	100 mV
Sensitivity	200 mV
Polarity	Selectable positive or negative
Drive	Selectable channel 1, channel 2 or both
Input Impedance	1 kΩ or 50 Ω (nom), DC coupled
Max toggle frequency	
12 bit mode	Sample clock output frequency divided by 320
14 bit mode	Sample clock output frequency divided by 240
Minimum pulse width	
Asynchronous timing between trigger/gate and sync clock output	1.1 * sync clock period
Synchronous timing between trigger/gate input and sync clock output	See set-up and hold timing under timing characteristics
Connector type	SMA

A common dynamic control input for both channels is provided on the front panel. The user can select, if the dynamic control input affects none, only channel 1/channel 2 only, or both channels. A detailed description of the dynamic control input including timing diagram and pin assignment is shown in the *M8190A User's Guide*.

Dynamic control input

Characteristics	**Description**
Input signals	Data[0..12]_In + Data_Select + Load [1]
Internal data width	19 bit, multiplexed using Data_Select
Data_Select	Data_Select = Low: Data[0..12] = Data[0..12]_In Data_Select = High: Data[13..18] = Data[0..5]_In
Number of addressable segments or sequences	2^{19} = 524 288
Data rate	DC to 1 MHz
Set-up time	3.0 ns (`Data[0..12]_In, `Data_Select' to rising edge of `Load')
Hold time	0.0 ns (rising edge of `Load' to `Data[0..12]_In, `Data_Select')
Minimum [3] latency [4]	Dynamic control input to direct out
12 bit mode	27520 sample clock cycles (meas)
14 bit mode	20640 sample clock cycles (meas)
Interpolation mode [5]	
Input range	
Low level	0 V to +0.7 V
High level	+1.6 V to +3.6 V
Impedance	Internal 1 kΩ pull-down resistor to GND
Connector	20 pin mini D ribbon (MDR) connector [2], cable Option 815

1. *`Data[0...12]'_In and `Data_Select' will be stored on rising edge of `Load signal.'*
2. *Manufacturer Part Number: N10220-52B2PC. Manufacturer: 3M.*
3. *As the current segment (or sequence or scenario) is always completed, the total latency is determined by the duration of the segment (or sequence or scenario). See characteristics of digital up-conversion if interpolation is enabled.*
5. *See characteristics digital up-conversion if interpolation is enabled.*

The M8190A can operate synchronously or asynchronously. Synchronous operation must be selected to achieve minimum delay uncertainty between Trigger Input, Event, Input or Dynamic Control Input and Direct Out or Marker Out. For synchronous operation Trigger/Gate Input, Event, Input or Dynamic Control must be synchronous to the Sync Clock Output.

Timing characteristics

Characteristics	Description
Setup time	
Trigger/gate in to rising edge of sync clock out	10.5 ns (typ)
Event in to rising edge of sync clock out	10.5 ns (typ)
Hold time	
Rising edge of sync clock out to trigger/gate in	–7.5 ns (typ)
Rising edge of sync clock out to event in	–7.5 ns (typ)
Delay in 12 bit mode	
Trigger/event in to direct/DC/AC out	10240 external sample clock cycles + 0.5 internal[1] sample clock cycles (nom)
Sync marker to direct/DC/AC out	0.5 internal[1] sample clock cycles - 4.9 ns (nom) (fSa >= 6.4 GSa/s) 0.5 internal[1] sample clock cycles - 8.0 ns (nom) (fSa < 6.4 GSa/s)
Delay in 14 bit mode	
Trigger/event in to direct/DC/AC out	7680 external sample clock cycles + 0.5 internal[1] sample clock cycles (nom)
Sync marker to direct/DC/AC out	0.5 internal[1] sample clock cycles - 4.9 ns (nom) (fSa >= 4.8 GSa/s) 0.5 internal[1] sample clock cycles - 8.0 ns (nom) (fSa < 4.8 GSa/s)
Sample marker to direct/DC/AC out	0.5 internal[1] sample clock cycles - 1.3 ns (nom)

1. Internal sample clock cycles. For definition of 'Internal sample clock cycles' refer to sample clock outputs specification.

Delay uncertainty

Asynchronous mode	
	64 external sample clocks in 12 bit mode
	48 external sample clocks in 14 bit mode
Synchronous mode	10 ps (typ) [2]

2. The delay accuracy in synchronous mode is equal to the peak-peak jitter between sync clock output and direct out.
Note: Timing characteristics of DUC, see digital up-conversion (DuC) chapter.

Variable Delay

In order to compensate for e.g. external cable length differences as well as the initial skew, channel 1 and channel 2 can be independently delayed with a very high timing resolution.

Setting the variable delay of channel 1 to 10 ps has following effect:

- Direct out1 (or amp out1, if selected) and sample marker out1 are delayed by 10 ps with respect to following signals: sample clock out, sync marker out1, sync marker out2, direct out2 (or amp out2, if selected), trigger/gate input, event input

Note: Modifying the variable delay of one channel always affects the delay of the analog output AND the sample marker of that channel.

The variable delay is split into two delay elements:

1. Fine delay
2. Coarse delay

The variable delay is the sum of fine delay and coarse delay. If a de-skew between channel 1 and channel 2 is needed, adjust in the first step the coarse delay to the optimum position. In the second step, use the fine delay to perfectly align both channels.

Variable delay

Characteristics	**Description**
Variable delay	Fine delay + coarse delay
Variable delay range	
$f_{Sa} \geq 6.25$ GSa/s	0 ps to 10.030 ns
2.5 GSa/s $\leq f_{Sa} <$ 6.25 GSa/s	0 ps to 10.060 ns
$f_{Sa} <$ 2.5 GSa/s	0 ps to 10.150 ns

Fine delay

The fine delay is independently adjustable for channel 1 and channel 2	
Delay range	
$f_{Sa} \geq 6.25$ GSa/s	0 ps to 30 ps
2.5 GSa/s $\leq f_{Sa} <$ 6.25 GSa/s	0 ps to 60 ps
$f_{Sa} <$ 2.5 GSa/s	0 ps to 150 ps
Delay resolution	50 fs
Accuracy	
$f_{Sa} \geq 6.25$ GSa/s	± 10 ps (typ)
2.5 GSa/s $\leq f_{Sa} <$ 6.25 GSa/s	± 20 ps (typ)
$f_{Sa} <$ 2.5 GSa/s	± 20 ps (typ)

1. For definition of "internal sample clock cycles", refer to sample clock output specification.
Note for delay in interpolation mode: Please see digital up-conversion specification.

Coarse delay

Characteristics	Description
The coarse delay is independently adjustable for channel 1 and channel 2	
Delay range	0 ps to 10 ns, variable
Delay resolution	
$f_{Sa} \geq 6.25$ GSa/s	10 ps
2.5 GSa/s $\leq f_{Sa} <$ 6.25 GSa/s	20 ps
$f_{Sa} <$ 2.5 GSa/s	50 ps
Accuracy	
$f_{Sa} \geq 6.25$ GSa/s	± 20 ps (typ)
2.5 GSa/s $\leq f_{Sa} <$ 6.25 GSa/s	± 20 ps (typ)
$f_{Sa} <$ 2.5 GSa/s	± 50 ps (typ)

When the variable delay is set to 0 ps, the channels operate in coupled mode and the same amplifier path for both channels is selected, the initial skew between channel 1 and channel 2 is 0 ps.

Initial skew between channel 1 and channel 2

Skew [1]	0 ps (nom)
Accuracy	± 20 ps (typ)

1. Coupling on, same amplifier path is selected for channel 1 and channel 2.

Reference clock output

Characteristics	Description
Source	Internal backplane 100 MHz
Frequency	100 MHz
Stability	± 20 ppm (see *M9502A/M9595A Data Sheet*)
Aging	± 1 ppm per year
Source	External REF CLK In
Frequency	100 MHz
Amplitude	1 V_{pp} into 50 Ω (nom)
Source impedance	50 Ω, AC coupled (nom)
Connector	SMA

Reference clock input

Input frequencies	Selectable 1 MHz to 200 MHz, in steps of 1 MHz
Lock range	± 35 ppm (typ)
Frequency resolution	1 MHz
Input level	100 mV_{pp} to 2 V_{pp}
Impedance	50 Ω, AC coupled (nom)
Connector type	SMA

Sync clock output

Frequency	
14 bit mode	Sample clock divided by 48 (sample clock source is always channel 1)
12 bit mode	Sample clock divided by 64 (sample clock source is always channel 1)
Interpolation mode	Sample clock divided by (24 x interpolation factor)
Output amplitude	1.0 V_{pp} (nom) into 50 Ω
Impedance	50 Ω nominal, AC coupled
Connector	SMA

Sample clock

There are two selectable sources for the sample clock:

- Internal synthesizer
- Sample clock input

The two channel instrument (Option 002) offers the flexibility to independently select the sample clock sources for channel one and channel two. If different clock sources are selected for the channels, both channels operate entirely independently with respect to sample rate and sequencing.

Internal synthesizer clock characteristics

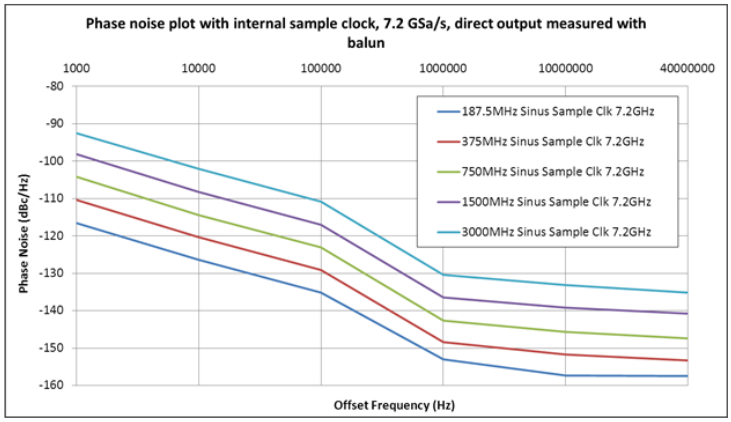
Characteristics	Description
Frequency	125 MHz to 12 GHz
Accuracy	± 20 ppm
Frequency resolution	15 digits, e.g. 10 µHz at 1 GHz
Phase noise [1]	f_{Sa} = 1 GHz < –110 dBc/Hz (typ) at 10 kHz offset, f_{out} = 125 MHz [2] f_{Sa} = 8 GHz < –105 dBc/Hz (typ) at 10 kHz offset, f_{out} = 1.0 GHz [2] f_{Sa} = 12 GHz < –105 dBc/Hz (typ) at 10 kHz offset, f_{out} = 1.5 GHz

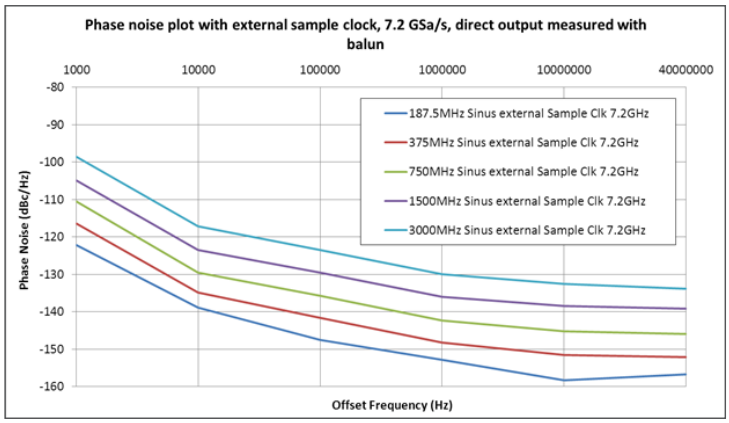
Sample clock input

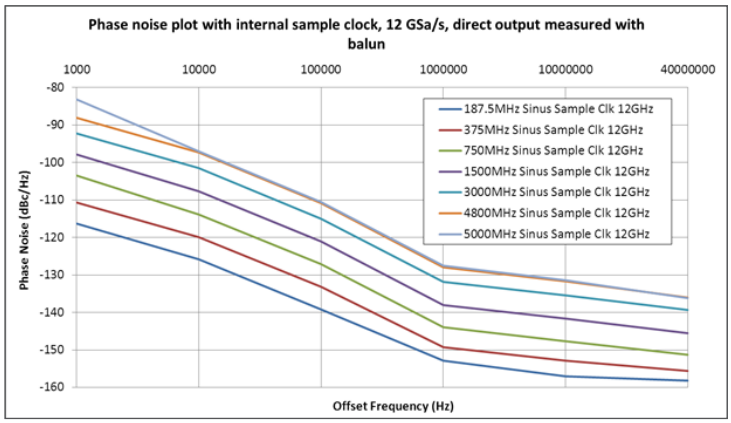
Frequency range [1]	1 GHz to 12 GHz
Input power range	+0 dBm to +7 dBm
Damage level	+8 dBm
Input impedance	50 Ω nom, AC coupled
Transition time	< 1 ns
Connector type	SMA

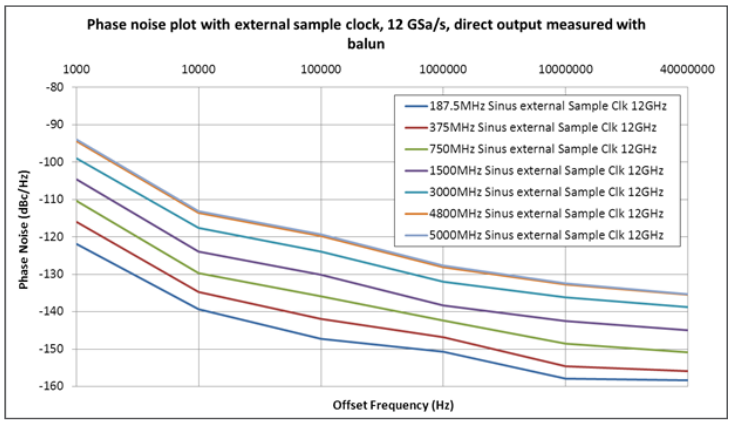
1. *The sample clock output is derived from the internal sample clock $f_{Sa, i}$. For $f_{Sa, i}$ = 500 MSa/s...1 GSa/s the sample clock output is twice of $f_{Sa, i}$. For $f_{Sa, I}$ = 250 MSa/s ... 500 MSa/s the sample clock output is four times $f_{Sa, i}$. For $f_{Sa, i}$ = 125 MSa/s ... 250 MSa/s the sample clock output is eight times $f_{Sa, i}$.*
2. *Measured at "data out".*

The M8190A allows very fine adjustments of the 2 channels. The plots show the phase noise using the delay adjustment.

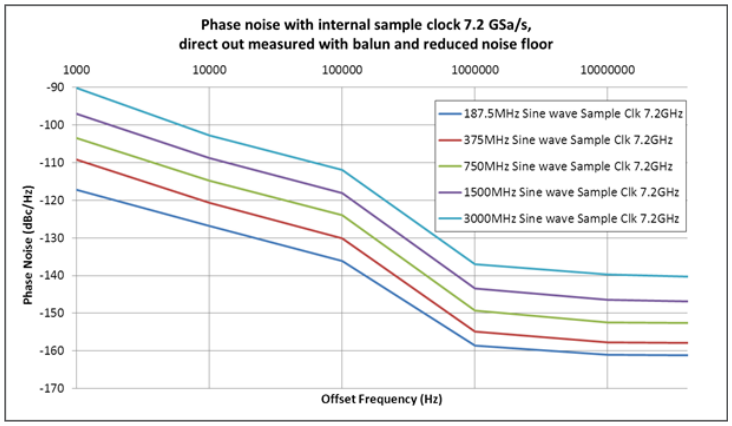


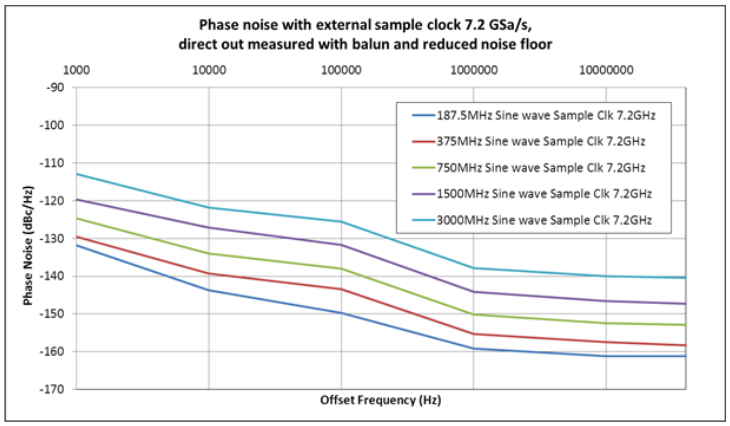


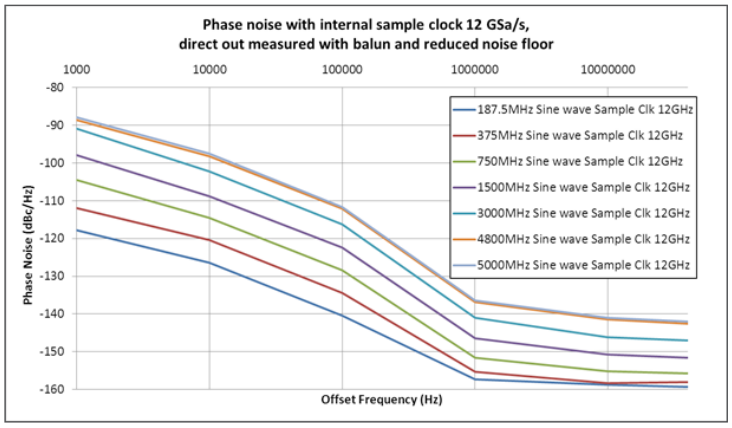


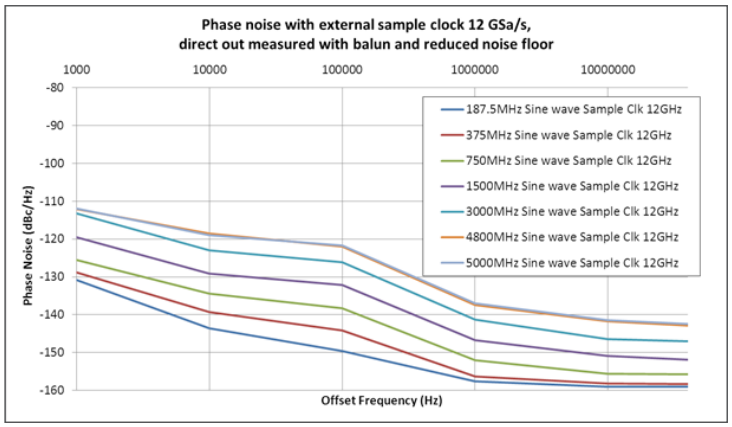


The M8190A allows very fine adjustments of the 2 channels. The plots show the phase noise not using the delay adjustment









The source for the sample clock output can be either the internal synthesizer or the sample clock input. The source for the sample clock output can be independently selected from the sample clock. For example, it is possible to operate the sample clock output from the internal synthesizer at f_1 to clock the DUT; as an example, f_1 may be divided by two by the DUT. In this case, $f_1/2$ can be connected to the sample clock input as to be used as the sample clock of the M8190A.

Sample clock output

Characteristics	Description
Source	Selectable, internal synthesizer or sample clock input
Frequency range [1]	1 GHz to 12 GHz
Output amplitude	400 mVpp (nom), fix
Input impedance	50 Ω (nom), AC coupled
Transition time (20% to 80%)	20 ps (typ)
Connector	SMA

The following table shows which sample clock out routings are possible if coupling is on.

Coupling = on			Channel 1			
			External clock		Internal clock	
			12 bit	14 bit	12 bit	14 bit
Channel 2	External clock	12 bit	External clock	—	—	—
		14 bit	—	External clock	—	—
	Internal clock	12 bit	—	—	Internal clock	—
		14 bit	—	—	—	Internal clock

The following table shows which sample clock out routings are possible if coupling is *off*.

Coupling = off			Channel 1			
			External clock		Internal clock	
			12 bit	14 bit	12 bit	14 bit
Channel 2	Channel 2 operate with external clock	12 bit	External or internal clock	External or internal clock	External or internal clock	External or internal clock
		14 bit	External or internal clock	External or internal clock	External or internal clock	External or internal clock
	Channel 2 operate with internal clock	12 bit	External or internal clock	External or internal clock	External or internal clock	—
		14 bit	External or internal clock	External or internal clock	—	External or internal clock

1. The sample clock output is derived from the internal sample clock $f_{Sa,\,i}$. For $f_{Sa,\,i}$ = 500 MSa/s...1 GSa/s the sample clock output is twice of $f_{Sa,\,i}$. For $f_{Sa,\,I}$ = 250 MSa/s ... 500 MSa/s the sample clock output is four times $f_{Sa,\,i}$. For $f_{Sa,\,i}$ = 125 MSa/s ... 250 MSa/s the sample clock output is eight times $f_{Sa,\,i}$.

Coupling between channel 1 and channel 2

The two channel instrument (Option 002) has two distinct modes of operation: coupling = off and coupling = on.

Coupling = off

- The two channels operate entirely independently
- The channels may run at different sample clock rates
- The channels may run from the same clock source (internal or external)
- The channels may operate from different clock sources (internal or external)
- The channels are being started asynchronously
- Following parameters can be changed individually per channel:
  - Frequency
  - Amplitude, offset
  - Amplifier path
  - Waveform
  - Sequence
  - Trigger mode (auto, triggered, gated)
  - Start/stop (programming/programming complete)
  - 12 bit or 14 bit mode
  - Dynamic sequencing on/off
- Following parameters can only be changed for both channels:
  - None

The following table shows which mode combinations are available, if coupling is *off*.

Coupling = off			Channel 1			
			External clock		Internal clock	
			12 bit	14 bit	12 bit	14 bit
Channel 2	External clock	12 bit	Available	Available	Available	Available
		14 bit	Available	Available	Available	Available
	Internal clock	12 bit	Available	Available	Available	—
		14 bit	Available	Available	—	Available

Coupling = on

- The two channels start synchronously; the clock source for channel 1 and channel 2 is the same
- The fix delay between channel 1 and channel 2 is the same
- Following parameters can be changed individually per channel:
  - Amplitude, offset
  - Amplifier path
  - Waveform
  - Sequence
  - Trigger mode
  - Variable delay
  - Dynamic sequencing on/off
- Following parameters can only be changed for both channels:
  - Frequency
  - Clock source internal or external
  - Start/stop (programming/programming complete)/abort
  - 12 bit or 14 bit mode
- Notes:
  - When changing from coupling = off to coupling = on, setting of above parameters from channels 1 are being transferred to channel 2
  - Following remote commands that are being sent to channel 1 (or ch2), affect channel 2 (or ch1) as well: frequency, bit mode, start/stop, trigger, event, dynamic segment/sequence select and enable
  - To allow full synchronous operation between channel 1 and channel 2, start/stop, trigger, event, dynamic segment/sequence select and enable always affect both channels; this is valid if the signals are generated at the hardware inputs or by software

The following table shows which mode combinations are available, if coupling is *on*.

Coupling = on			Channel 1			
			External clock		Internal clock	
			12 bit	14 bit	12 bit	14 bit
Channel 2	External clock	12 bit	Available	—	—	—
		14 bit	—	Available	—	—
	Internal clock	12 bit	—	—	Available	—
		14 bit	—	—	—	Available

Internal trigger generator

Characteristics	Description
Frequency range	100 mHz to f_{max}
f_{max}	Sync clock out frequency divided by 5 e.g.: 12 bit mode, f_{Sa} = 12 GHz: f_{max} = 12 GHz/64/5 = 37.5 MHz e.g.: 14 bit mode, f_{Sa} = 8 GHz: f_{max} = 8 GHz/48/5 = 33.3 MHz
Frequency resolution	100 mHz

SEQUENCER

The standard configuration of the M8190A offers:

- Continuous, self armed mode with one segment
- Triggered, self armed with one segment
- Gated, self armed with one segment

Sample memory Standard Option 02G 12 bit mode Option 02G 14 bit mode	 128 MSa per channel 2048 MSa per channel 1536 MSa per channel
Option SEQ offers the enhanced sequencing functionality described below	
Minimum segment length	320 samples in 12 bit mode; 240 samples in 14 bit mode
Waveform granularity	64 samples in 12 bit mode; 48 samples in 14 bit mode
Segments	1 to 512 k (2^{19}) unique segments The maximum length of a segment can be up to 2048 MSa. A single segment can consist of multiple sections that are downloaded individually to the instrument and are linked inside the M81190A to form a segment.
Segment loops	A total of 4 billion (2^{32}) loops can be defined for each segment
Sequences	Up to 512 k (2^{19}) total unique waveform sequences can be defined. A sequence is a continuous series of segments.
Sequence table entries	Up to 512 k segment table entries can be defined as the sum of entries for all sequence tables
Sequence loops	A total of 4 billion (2^{32}) loops can be defined for each sequence
Scenarios Scenario table entries	Up to 512 k (2^{19}) scenarios can be defined. A scenario is a continuous series of sequences Up to 512 k (2^{19}) loop can be defined for each scenario Each sequence in a scenario can be looped up to 4 billion (2^{32}) times. Switching between different scenarios is controlled by software.
Dynamic scenario control	A parallel input bus is used to externally switch between scenarios. Jumps between scenarios can be immediate (current scenario is interrupted) or synchronous (current scenario is completed before jumping to the next scenario).

DIGITAL UP-CONVERSION

In a two-channel instrument, each channel has a separate digital up-conversion engine. All parameters (e.g. carrier frequency, amplitude, waveforms, etc.) can be set independently. If the two channels are used in "coupled" mode, they are fully phase coherent.

Characteristics	**Description**	
Sampling rate	1000 MSa/s – 7200 MSa/s	
Carrier frequency		
Range	0 Hz ... 12 GHz (observe frequency response and sin x/x roll-off)	
Resolution	Sample clock/2^{72}	
Phase range	0 – 360°	
Phase resolution	0.002°	
Amplitude range	0 to 100%	
Amplitude resolution	20,000 steps	
Frequency sweep rate	2 Hz/hour to 40 GHz/µs	
Sample memory		
Depth	768 M IQ sample pairs	
Granularity	24	
Minimum segment length for data segments	120 IQ pairs	
Minimum segment length for configuration segments	240 IQ Pairs	
Vertical resolution IQ	15 bit samples for I and Q	
Vertical resolution DAC	14 bit independent of 12 bit mode and 14 bit mode	
Interpolation factors	x3, x12, x24, x48	
SFDR and harmonics	See specs in 14 bit mode	
Mode dependent modulation bandwidth Interpolation factor	Max. input sample rate	Max. modulation bandwidth
x3	2400 MSa/s	1920 MHz
x12	600 MSa/s	480 MHz
x24	300 MSa/s	240 MHz
x48	150 MSa/s	120 MHz
Modulation bw ripple	0.8 x Fs, where Fs is the input I/Q sample rate, max 1 dB	
Delay (fSa = 1 GSa/s to 7.2 GSa/s)		
Trigger/event in to direct out	Interpolation factor [1] * 3840 external sample clock + 4.5 internal[1] sample clock cycles – 5.3 ns (nom)	
Trigger/event in to DC out	Interpolation factor [1] * 3840 external sample clock + 4.5 internal[1] sample clock cycles – 4.6 ns (nom)	
Trigger/event in to AC out	Interpolation factor [1] * 3840 external sample clock + 4.5 internal[1] sample clock cycles – 4.5 ns (nom)	
Delay sync marker out to direct out	4.5 internal [1] sample clock cycles – 8.0 ns (nom)	
Delay sample marker out to direct out	–1.3 ns + 4.5 internal sample1 clock cycle (typ)	
Sync clock output	Sample clock divided by (24 x interpolation factor)	
Minimum latency	Interpolation factor * 10320 sample clock cycles (meas)	
Trigger/gate and event input		
Maximum toggle frequency	Sample clock output frequency divided by (120 * interpolation factor)	

1. Internal sample clock cycles. For definition of "internal sample clock cycles" refer to sample clock output specifications.

Marker		
Characteristics	**Description**	
Sync marker		
Timing resolution	24 input IQ sample pairs	
Width	Multiples of 24 input IQ sample pairs	
Sample marker		
Timing resolution	1 input IQ sample pair	
Width	Interpolation factor	Width in DAC output samples
	x3	24
	x12	24
	x24	24
	x48	48
Sample marker output delay	Marker to data is 3.5 sample clock cycles	

Memory management	
The IQ baseband waveform and waveform attributes such as carrier frequency, phase, and amplitude are stored independently. Thus, repetitive waveforms with different attributes can be stored much more efficiently. Attributes are stored in tables. The sequencer connects waveform and its attributes at runtime. Carrier frequency and amplitude can also be controlled by software.	
Table sizes	
Amplitude table	32 k
Frequency table	32 k
Action table	32 k
Actions include: set carrier frequency, set amplitude, set phase, reset phase, phase bump, set sweep rate, sweep run, sweep stop	

General

Characteristics	Description
Power consumption	210 W (nom, 12 GSa/s operation)
Operating temperature	0 °C to 40 °C
Operating humidity	5% to 80% relative humidity, non-condensing
Operating altitude	Up to 2000 m
Storage temperature	–40 °C to 70 °C
Stored states	User configurations and factory default
Power on state	Default
Interface to controlling PC	PCIe (see AXIe chassis specification)
Form factor	2-slot AXIe
Dimensions (WxHxD)	60 mm x 322.5 mm x 281.5 mm
Weight	4.9 kg
Safety designed to	IEC61010-1, UL61010, CSA22.2 61010.1 certified
EMC tested to	IEC61326
Warm-up time	30 min
Calibration interval	1 year recommended
Warranty	3 years standard

Cooling requirements

When operating the M8190A choose a location that provides at least 80 mm of clearance at rear, and at least 30 mm of clearance at each side.

Download times

Download times: Using IVI-COM driver	
1 M samples	3 ms (meas)
128 M samples	350 ms (meas)
512 M samples	1.4 s (meas)
2 G samples	6 s (meas)

DEFINITIONS

Specification (spec)	The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 °C to – 40 °C and after a 45-minute warm up period. Within ± 10 °C after autocal. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.
Typical (typ)	The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).
Nominal (nom)	The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23 °C).
Measured (meas)	An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23 °C).
Accuracy	Represents the traceable accuracy of a specified parameter. Includes measurement error and timebase error, and calibration source uncertainty.

SOFTWARE

Operating systems	Supported operating system is • Microsoft® Windows® XP 32 bit • Microsoft Windows Vista® 32 bit • Microsoft Windows Vista 64 bit • Microsoft Windows 7 32 bit • Microsoft Windows 7 64 bit
Soft front panel	A graphical user interface (GUI or soft front panel) is offered to control all functionality fo the instrument. It contains screens for controlling clock, outputs, marker, trigger, sequencer, importing waveforms and creating standard waveforms.
SCPI language	Remote control via SCPI
IVI-driver	An IVI-COM driver as well as IVI-C driver will be provided

The Modular Tangram

The four-sided geometric symbol that appears in this document is called a tangram. The goal of this seven-piece puzzle is to create identifiable shapes—from simple to complex. As with a tangram, the possibilities may seem infinite as you begin to create a new test system. With a set of clearly defined elements—hardware, software—Agilent can help you create the system you need, from simple to complex.

Challenge the Boundaries of Test

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