Specifications

 This appendix lists *gigaBERT700* Generator and Analyzer specifications.

Generator Specifications

Internal Clock Source

Frequency range	150 kHz to 705 MHz
Resolution	1 kHz
Stability	10 ppm
Number of frequency memories	10

External Clock Input

Frequency range	DC to 705 MHz
Input level	500 mV to 1.4 V p-p
Impedance	50 ohms, AC-coupled
Connector	SMA

Data Outputs

Amplitude	variable, 500 mV to 2.0 V in 50 mV steps
Baseline offset	variable, -2.0 V to +1.8 V, in 50 mV steps
Pulse top limit	+2.8 V into 50 ohms
	+5.6 V into an open load
Rise/fall times (20 to 80%)	150 ps (typical) when amplitude equals 1 V
Jitter	100 ps p-p max., referenced to EXT CLK
Source impedance	50 ohms
Output timing	CLOCK and DATA are edge aligned, ± 100 ps
Connectors	SMA
Data Inhibit	rear-panel SMA, ECL (50 ohms to -2 V term.)
Data inhibit rate	asynchronous, 1 bit + 500 ps minimum width
Data invert	front panel select

Clock Outputs

Format	true and compliment
Amplitude	variable, 500 mV to 2.0 V, in 50 mV steps
Baseline offset	variable, -2.0 V to +1.8 V, in 50 mV steps
Pulse top limit	+2.8 V into 50 ohms
	+5.6 V into an open load
Rise/fall times (20 to 80%)	200 ps (typical) when amplitude equals 1 V.
Jitter	100 ps p-p max., referenced to EXT CLK
Source impedance	50 ohms
Connectors	SMA

Error Injection

Internal rates	single or 1E-n, n = 4, 5, 6, or 7
External error input	ECL, 50 ohms to -2V, 1 error per rising edge
External injection rate	50 ns minimum pulse width
External error connector	SMA

Auxiliary Outputs (Clock/4, Pattern Sync)

Level	200 mV p-p into 50 ohms, 400 mV into high impedance
Impedance	50 ohms
Clock/4 output	system clock / 4, toggles on rising edge of system clock
Pattern sync. pulse (PRBS)	high for 1 bit per frame
Pattern sync. pulse (16 bit words)	low for first byte, high for second byte, etc.
Pattern sync. pulse (long-words)	high for one byte each frame; location is user-programmable
Connectors	SMA

RS-232C and GPIB Interfaces

Controlled functions	all front panel functions except PANEL LOCK and POWER.
Read-back functions	all results and all settings except for PANEL LOCK
GPIB terminator character	LF (line feed) = 0A hex
GPIB address	Front panel select 0 - 30

AC Power Requirements

Voltage range	90 to 250 VAC, auto-ranging
Frequency range	47 to 63 Hz
Power	125 VA max.
Fuse rating	115 VAC, 2 A, or 230 VAC, 1 A
Operating temperature range	0 to 50 degrees C

Mechanical

Weight	10 Kg (22 lb.)
Size	152H x 366W x 340D mm (6" x 14.4" x 13.4")

Analyzer Specifications

Clock Inputs

Format	Differential or single-ended
Frequency range	150 kHz to 705 MHz
Input level	500 mV to 6.0 V p-p
Input threshold	variable, -3.00 V to +4.50 V, in 50 mV steps
Impedance	50 ohms
Termination voltage	selectable, GND, -2 V, +3 V, or AC

Data Inputs

Format	NRZ-L, true or inverted, differential or single-ended
Input threshold	variable, -3.0 V to + 4.5 V in 50 mV steps
Input amplitude	500 mV to 6.0 V p-p
Termination voltage	selectable, GND, -2 V, +3 V, or AC
Impedance	50 ohms
Delay relative to clock	variable: 0 to 4.00 ns in 20 ps steps
Connectors	SMA

Reference Data Input

Format	NRZ-L true
Input threshold	variable: -2.0 V to +1.0 V in 50 mV steps
Input amplitude	500 mV to 6.0 V p-p
Termination voltage	selectable: GND, -2 V, +3 V, or AC
Impedance	50 ohms
Delay relative to clock	variable: 0 to 4.00 ns in 20 ps steps
Connector	SMA

Auxiliary Monitor Outputs (Data, Clock, and PSYNC)

Amplitude	250 mV p-p into 50 ohms, 500 mV into a high impedance
Output impedance	50 ohms
Data monitor	Latched input data
Clock monitor	Buffered input clock
Pattern sync.	1 bit-wide pulse per frame
Error inhibit	Rear-panel, ECL
Error Output	Real-panel, ECL
Connectors	SMA

Auto_Search and Pattern Synchronization

Auto-Search. When Auto_Search is on (enabled) the Analyzer automatically sets input Data Threshold, input Data Delay (relative to clock input signal), input pattern (PRBS or 8/16 bit word pattern), and data polarity (inverted or non-inverted). When Auto_Search is off (disabled) set up of these parameters is manual.

(Pattern) Synchronization Disable. When Sync. Disable is off, the Analyzer will try to re-synchronize the pattern detector when BER goes above the current synchronization threshold by looking for a new pattern frame alignment. When Sync Disable is on, this process is disabled.

Synchronization Thresholds

PRBS patterns	25% (1024 errors/4096 bits)
Word patterns (8/16 bit)	3.1% (128 errors/4096 bits)
Word patterns (128K option installed)	programmable (See Table A-1)

Table A-1 Synchronization Thresholds With 128K Option Installed

Sync. Level	BER	Errors/bits
1	3.1E-2	256/8192
2	7.8E-3	256/32768
3	1.9E-3	256/131072
4	9.7E-4	256/262144
5	4.8E-4	256/524288
6	2.4E-4	256/1048576
7	1.2E-4	256/2097152
8	6.1E-5	256/4194304
9	3.0E-5	256/8388608

Measurements

BER - three simultaneous: Totalize, Window, and Test, displayed as 9.9E-01 to <1.0E-16

Total bit errors - three simultaneous: Totalize, Window, and Test, displayed as 0 to 99999999

Totalize mode - BER/bit errors since last power-on or clear

Window mode - BER/bit errors over a sliding window. Programmable in terms of time (1 sec - 24 Hrs) or bits (1.0E+8 to 1.0E+16).

Test mode- BER/bit errors and other measurements over untimed, timed (1 sec - 24 Hrs) or repeat intervals.

Additional Test Mode Measurements - Includes: ES, EFS, TES, SES, DM, US, and LOS (See Chapter 5).

Frequency - Input clock frequency, 10 kHz resolution

History indicators - (Pattern) Sync. Loss, Bit Error, Phase Error, Power (Loss).

RS-232C and GPIB Interfaces

Controlled functions - all front panel functions except PANEL LOCK and POWER.

Read-back functions - all results and all settings except for PANEL LOCK

GPIB terminator character - LF (line feed) = 0A hex

GPIB address - Front panel select 0 - 30

Printer (Parallel) Interface

Format - Parallel; compatible with parallel (LPT:) ports on ISA personal computers.

Reports - Analyzer Settings, End-of-Test, On-Error, End-of-Window, On Demand Test Summaries (See Chapter 5 for details).

AC Power Requirements

Voltage range - 90 to 250 VAC, auto-ranging

Frequency range - 47 to 63 Hz

Power - 125 VA max.

Fuse rating - 115 VAC, 4 A, or 230 VAC, 2 A

Operating temperature range - 0 to 50 degrees C

Mechanical

Weight - 10 Kg (22 lb.)

Size - 152H x 366W x 340D mm (6" x 14.4" x 13.4")

Low Voltage Declaration

Category	**Standard**
EC Declaration of Conformity - Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities: EC Council Directive 89/336/EC Low Voltage Directive 73/23/EEC EN61010-1/A1 - Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use.

Pattern Specifications (Generator and Analyzer)

Data Patterns

Format - NRZ-L, normal and compliment

PRBS patterns - 2^n-1, n = 7, 15, 17, 20, 23

Word pattern length - 16 bits (128 K bits optional)

Word pattern bit order - LSB or MSB first

Number of word pattern memories - 8, plus the current word

PRBS Pattern Phase Tap Information

The PRBS patterns used in the *gigaBERT700* Generator and Analyzer are generated by a shift-register and exclusive OR feedback technique. The pattern is dependent on which feedback taps (shift register outputs) are selected.

For example, PN7 is defined to be a seven-stage shift register, with the output of stages 6 and 7 fed back (through an exclusive OR gate) to the input of stage one of the shift register. The feedback taps used in *gigaBERT700* Generator and Analyzer PRBS circuits are listed below:

Pattern	**Feedback Taps**
PN 7	6 and 7
PN15	14 and 15
PN17	14 and 17
PN20	17 and 20
PN23	18 and 23